Digitally-Assisted Leakage Current Supply Circuit for Reducing the Analog LDO Minimum Dropout Voltage

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***Abstract*—A digitally-assisted leakage current supply (LCS) circuit reduces the maximum current demand for analog low-dropout (LDO) voltage regulators to lower the minimum dropout voltage ($V_{DO,MIN}$), and consequently, enable a wider range of LDO operation for power savings in system-on-chip processor cores. From silicon measurements in a 130nm test chip, the LCS assisted hybrid LDO decreases $V_{DO,MIN}$ by 30-38%, resulting in core power reduction of 21-28% at equal clock frequencies within the wider LDO operating range.**

Keywords—LDO, Dynamic Voltage and Frequecny Scaling, Voltage Headroom, Leakage Current Sensor

I. INTRODUCTION

Industrial system-on-chip (SoC) processors contain a number of distinct supply voltage (V_{DD}) rails driven from a power management integrated circuit (PMIC). A cluster of SoC processor cores share the same V_{DD} and clock frequency (F_{CLK}) from a dedicated phase-locked loop (PLL). Each core in a cluster must either operate at the same V_{DD} and F_{CLK} as the other cores in the cluster or disable operation with a power gate configuration. With on-die low-dropout (LDO) voltage regulators [1-8], each cluster on a shared voltage rail may employ a unique V_{DD} and F_{CLK}. In this case, the cluster requiring the highest V_{DD} and F_{CLK} determines the shared V_{DD} rail. A cluster with a lower target V_{DD} and F_{CLK} always operates at the lower F_{CLK} for a linear F_{CLK} power reduction. If this cluster satisfies the LDO minimum dropout voltage ($V_{DO,MIN}$) requirement, this cluster executes at the lower target V_{DD} via LDO mode for an additional linear V_{DD} power reduction, which accounts for the LDO power loss. The dual-core design in Fig. 1 represents two separate clusters on a shared voltage rail (V_{IN}) with each cluster containing a unique core, F_{CLK} generator, and power management unit (PMU).

Premium-tier SoC CPU cores typically prefer analog LDOs to satisfy the high-bandwidth requirements for fast transient performance. Area-constraints on the size of the power PFET (i.e., transistor M_{PA} in the PMU in Fig. 1) typically limits the current drive in an analog LDO and results in higher $V_{DO,MIN}$. The $V_{DO,MIN}$ values of high-bandwidth analog LDOs range from 150-300mV in order to supply the core maximum current demand at the worst-case dynamic and leakage power conditions [3, 4]. A key challenge in industrial analog LDOs is this large $V_{DO,MIN}$, which limits the opportunities to enable LDO mode for voltage scaling power benefits.

In recent years, all-digital LDOs have received significant attention to address the $V_{DO,MIN}$ issue [1, 2, 6]. While digital LDOs have a lower $V_{DO,MIN}$ requirement as the power PFETs operate in the linear region, these designs suffer from low gain and high output ripple due to limit cycle oscillations [1]. Hence, high-bandwidth analog LDOs are preferred in high-performance cores as compared to digital LDOs. Recently, hybrid LDOs [5, 7] employ both digital and analog loops to trade-off the strengths and weaknesses of traditional digital and analog designs. The challenge with the hybrid LDO designs is managing the complex current-load sharing between the analog and digital loops while maintaining high-bandwidth and stability. The load sharing problem often leads to an overdesign of both the analog and digital loops. This paper describes a digitally-assisted leakage current supply (LCS) circuit and 130nm test-chip measurements to reduce the maximum current demand for analog LDOs. The low-bandwidth LCS circuit supplies the slow-changing leakage current and the high-bandwidth analog LDO supplies the fast-changing dynamic current. By decreasing the maximum current requirement for the analog LDO, the LCS reduces the analog LDO $V_{DO,MIN}$, resulting in core power savings.

II. TEST-CHIP DESIGN

The block diagram in Fig. 1 captures the behavior of an industrial SoC with two cores on a shared voltage rail with each core containing a separate F_{CLK} generator and PMU to allow unique core voltage (V_{CORE}) and F_{CLK} operation. The PMU in Fig. 1 consists of header switches (HS), an analog LDO, and an LCS circuit to allow four configurations as described in Table 1. (1) Power gate mode with the analog LDO and HS disabled, (2) HS mode with the analog LDO disabled and HS enabled to

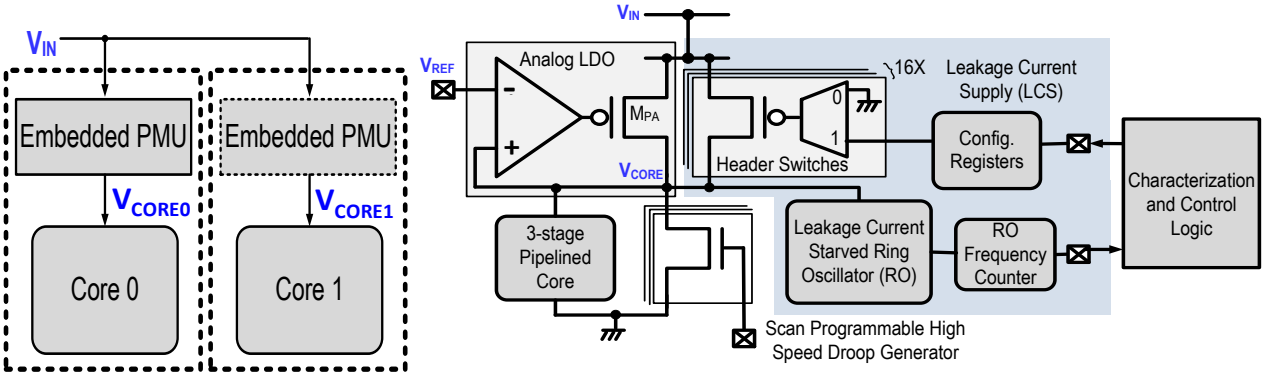

Fig 1: Test-chip architecture of a dual core voltage (V_{CORE}) design on a shared voltage rail (V_{IN}) and power management unit (PMU) block diagram with header switches (HS), analog LDO and the leakage current supply (LCS) circuit.

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Power Modes	Design Choice	Analog LDO	Header Switches (HS)
Power Gated	Baseline & Proposed	OFF	OFF
HS Mode: $V_{CORE}=V_{IN}$	Baseline & Proposed	OFF	ON
LDO Mode: $V_{CORE} \leq V_{IN}-V_{DO,MIN}$	Baseline	ON	OFF
	Proposed	ON	LCS Assisted Hybrid LDO

Table 1: Power management unit (PMU) configurations.

LDO Characterization	Dominant Pole Location	
	Internal	Output
V_{DROOP}	High	Low
Power Supply Rejection	Low	High
Unity Gain Bandwidth	Low	High
Light Load Stability	No	Yes
On chip Integration	Standard	Difficult

Table 2: Comparison between output-pole and internal-pole dominated analog LDOs.

directly connect V_{CORE} to V_{IN}, (3) LDO mode in the baseline design with LDO enabled and HS disabled, and (4) LDO mode in the proposed design with LDO enabled and the LCS circuit controlling the HS transistors. In the LDO mode for the proposed design, the LCS circuit supplies the slow-changing leakage current while the high-bandwidth analog LDO supplies the fast-changing dynamic current. By decreasing the maximum current requirement for the analog LDO, the LCS lowers the analog LDO $V_{DO,MIN}$ while keeping the power PFET (M_{PA}) in saturation, thus increasing the opportunities to enable LDO mode for core power reduction.

An alternative approach to reduce the headroom is to increase the width of the power PFET (M_{PA}). This leads to a larger PMU area and degrades the loop dynamics in both internal-pole and output-pole dominant analog LDO loops. As described in Table 2, if the analog LDO is output-pole dominant, then a wider M_{PA} shifts the internal pole at the gate of M_{PA} to a lower frequency, thereby reducing the phase margin. Conversely, if the analog LDO is internal-pole compensated, then a wider M_{PA} reduces the loop bandwidth, thus negatively affecting the response time to large load steps. To address these issues, the proposed LCS circuit enables a lower $V_{DO,MIN}$ while minimizing the impact on the area and the analog loop dynamics. In the proposed design, the LCS circuit supplies a portion of the load current. This is particularly effective at high temperatures when the leakage current, and hence, the total load current is the highest. Due to load sharing, the analog power PFET (M_{PA}) is smaller, thus decreasing the gate capacitance and allowing a higher frequency pole compared to a baseline analog-only design. As a result, the proposed design fully integrates an output-pole dominant, capacitor-less analog LDO with superior performance as summarized in Fig. 2.

From Fig. 1, load sharing through the HS devices is enabled by the LCS circuit. The LCS circuit includes: (1) Leakage-current-starved ring oscillator (RO), as described in Fig. 2, to monitor the changes in core leakage across temperature (T) and process variation, (2) RO frequency counter to map the RO frequency output (F_{RO}) to a digital signature over a programmable period of time (e.g., 1ms), and (3) Control logic that receives the digital signature to enable a target number of HS transistors to supply the load leakage current. The LCS leakage-current-starved RO contains an NFET footer device with a control voltage (V_{CNTL}) biased below the NFET threshold voltage (V_{TH}). From silicon measurements, a V_{CNTL} of 200mV ensures the voltage discharge of the internal RO nodes is governed by the NFET leakage current to allow the RO frequency (F_{RO}) to track leakage current while maintaining a sufficiently high F_{RO} to allow leakage monitoring and LCS configuration every 1ms. The control logic requires post-silicon characterization to determine the configuration register settings. An external on-board circuit

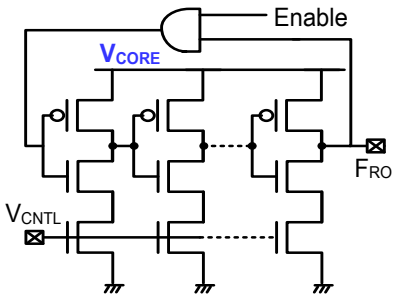


Fig 2: LCS leakage-current-starved ring oscillator (RO) schematic with $V_{CNTL} < V_{TH}$.

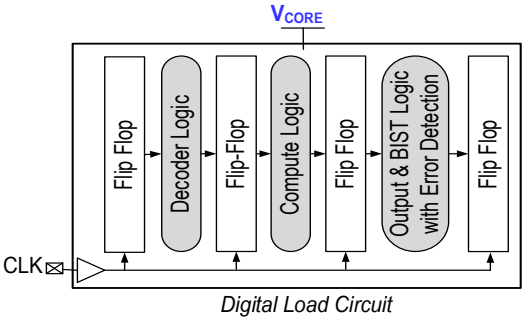


Fig 3: Three-stage pipeline prototypical core.

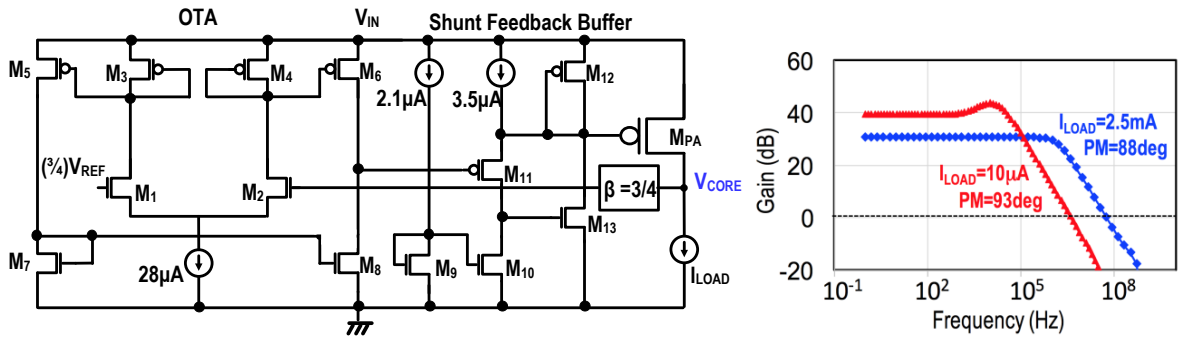
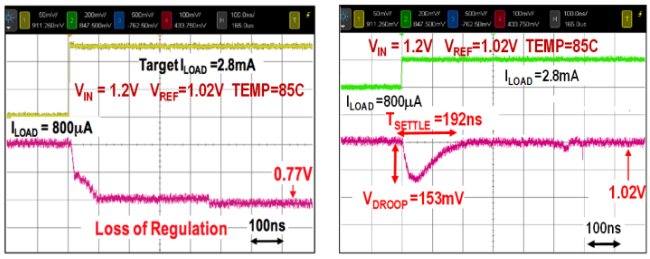


Fig 4: Output-pole dominant two-stage analog LDO schematic and simulated LDO loop gain for heavy and light load conditions.



(a) (b)

Fig 5. Measured oscilloscope captures after a load step for (a) analog LDO, which fails to regulate, and (b) LCS assisted hybrid LDO, which continues to regulate.

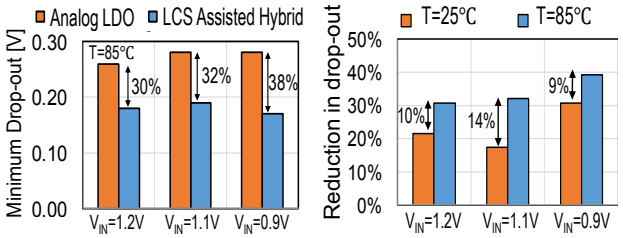


Fig. 6: Measured minimum dropout voltage ($V_{DO,MIN}$) for analog LDO and LCS assisted hybrid LDO as well as LCS assisted hybrid LDO $V_{DO,MIN}$ reduction across temperature versus V_{IN}

contains the control logic and provides the interface for silicon characterization. The test-chip contains a three-stage pipeline circuit in Fig. 3 with built-in self-test to mimic core functionality and scan programmable NFETs to generate realistic load steps.

The output-pole dominant analog LDO in Fig. 4 features a two-stage error amplifier design, consisting of an operational transconductance amplifier (OTA) stage with a low-output capacitance followed by a shunt feedback stage with a low-output resistance. This places the internal poles of the system at high frequencies (i.e., 100s of MHz), which is well beyond the unity gain bandwidth of the loop. The dominant pole of the analog amplifier is at the output node (V_{CORE}). Even with a small load capacitance of 400pF and no external capacitance, the worst-case phase margin is simulated at 88°. Excellent light load stability allows the analog LDO to provide retention voltage to the load circuits, when state preserving flip-flops consume ~100µA of total current.

III. Measurement Results

Measured oscilloscope captures in Fig. 5 with V_{IN}=1.2V, T=85°C, and a dropout of 180mV demonstrate that the baseline design fails to regulate under a load step, whereas the LCS

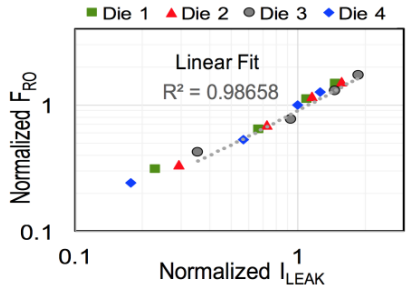


Fig. 7: Measured LCS leakage-current-starved RO frequency (F_{RO}) versus core leakage current (I_{LEAK}) with temperature ranging from 25°C to 85°C for each die.

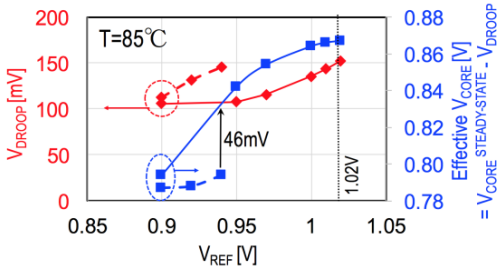
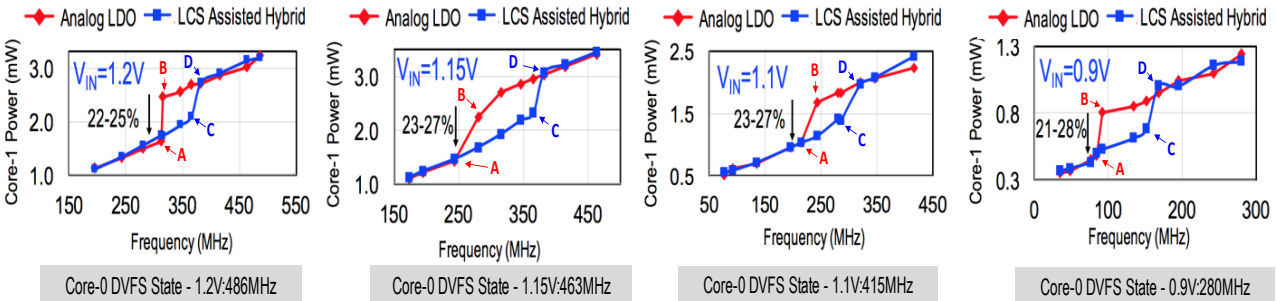


Fig. 8: Measured voltage droop (V_{DROOP}) and effective V_{CORE} versus V_{REF} for a load step from 0.8mA to 2.8mA. (Dotted Lines: Analog LDO, Solid Lines: LCS assisted hybrid LDO)

assisted hybrid LDO continues to regulate. In comparison to the analog LDO, measurements in Fig. 6 reveal that the LCS assisted hybrid LDO reduces $V_{DO,MIN}$ by 30-38% for three different V_{IN} values. The efficacy of the LCS assisted hybrid LDO is most pronounced at high T (85°C), where leakage is high, providing an additional 9-14% $V_{DO,MIN}$ reduction relative to the analog LDO as compared to T=25°C.

From measurements in Fig. 7 across four dies and T ranging from 25-85°C, the leakage sensor F_{RO} closely tracks the changes in core leakage current. For an industrial SoC processor, this data indicates that post-silicon characterization of a relatively small number of parts (e.g., 100s) across wide ranges of T can provide the configuration register settings for the LCS control logic for every part in high-volume shipping, thus avoiding the expensive test time of per part calibration. Detailed transient measurements in Fig. 8 of the proposed design as compared to the analog LDO at V_{IN}=1.2V and T=85°C with a load step from 800µA to 2.8mA demonstrate: (1) Voltage droop (V_{DROOP}) becomes worse in both designs as the reference voltage (V_{REF}) increases due to the diminishing



(a) (b) (c) (d)

Fig 9. Measured Core1 power versus clock frequency across multiple dynamic voltage-frequency scaling (DVFS) states with Core0 setting V_{IN}. "A" and "C" represent the maximum V_{CORE1} while satisfying $V_{DO,MIN}$ for the analog LDO and LCS assisted hybrid LDO, respectively. "B" and "D" represent the switch to HS mode for the analog LDO and LCS assisted hybrid LDO, respectively.

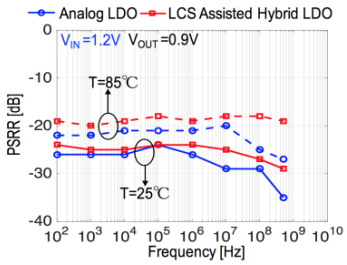


Fig 10: Measured power supply rejection ratio.

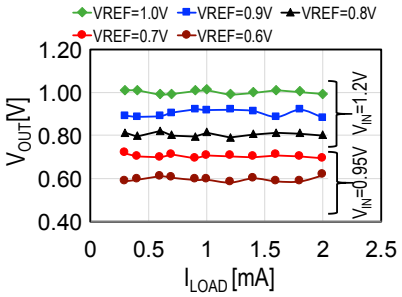


Fig 11: Measured load regulation.

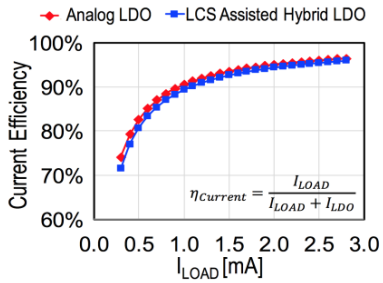
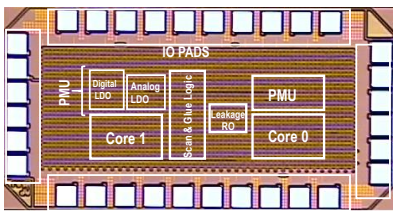


Fig 12: Measured current efficiency.

loop gain, (2) Analog LDO regulates until 0.94V, whereas the LCS assisted hybrid LDO operates until 1.02V, thus providing an extended operating range, and (3) Effective core voltage (V_{REF}-V_{DROOP}) is 46mV higher in the proposed design at V_{REF}=0.94V, translating to lower V_{DD} or F_{CLK} guardbands.

In measuring the impact of the LCS assisted hybrid LDO on digital loads in Fig. 9, Core0 operates at highest V_{DD} and F_{CLK}, and thus, determines V_{IN}. Core0 V_{IN}:F_{CLK} values are 1.2V:486MHz, 1.15V:463MHz, 1.1V:415MHz, and 0.9V:280MHz. Core1 executes at the lower F_{CLK}. If V_{IN}-V_{CORE1} ≥ $V_{DO,MIN}$, then Core1 operates at the lower V_{DD} via LDO mode to support the Core1 F_{CLK}; otherwise V_{CORE1} remains connected to V_{IN} in HS mode. Each plot in Fig. 9 contains four distinct operating points ("A"-"D"). For the baseline design, "A" represents the maximum V_{CORE1} (i.e., maximum F_{CLK} in LDO mode) in which the analog LDO satisfies $V_{DO,MIN}$ while maintaining regulation and "B" indicates the necessary switch to HS mode. For the proposed design, "C represents the maximum V_{CORE1} in which the LCS assisted hybrid LDO satisfies $V_{DO,MIN}$ while maintaining regulation and "D" indicates the switch to HS mode. The $V_{DO,MIN}$ reduction from the LCS assisted hybrid LDO enables a wider range of LDO operation, as defined from point "A" to point "C" in Fig. 9, thus resulting in new V_{CORE1}:F_{REF} DVFS states. The availability of these new DVFS states results in core power reduction of 21-28% at iso-F_{CLK} within this range. From power supply rejection ratio (PSRR) measurements in Fig. 10, the additional LCS PFET shunt devices in parallel with the analog LDO has a small effect on the loop gain. The PSRR plot also demonstrates: (1) High overall bandwidth and (2) No peaking effect, which is consistent with an output-pole dominant analog LDO design. Load regulation in Fig. 11 is less than 1mV/mA and peak current efficiency in Fig. 12 is 97.2%. The LCS circuits are duty cycled and operated every 1ms, resulting in a small decrease in the overall current efficiency. A comparison in Table 3 with state-of-the art designs indicate competitive FOMs and low $V_{DO,MIN}$ as compared to traditional analog LDO solutions. Fig. 13 describes the chip micrograph and characteristics.



Process	GF 130nm 8M-CMOS
Package	QFN
Core Area	0.0758 mm²
LDO+Header Area	0.0163 mm²
V_{IN}	0.9V-1.2V
V_{OUT}	0.6V-1.02V

Chip Characteristics

Fig.13 Test-chip micrograph and characteristics.

	This Work	[4]	[3]	[1]	[2]
Technology	130nm	28nm	65nm	130nm	28nm
LDO Type	**Hybrid**	**Analog**	**Analog**	**Digital**	**Digital**
V_{IN} (V)	0.9-1.2	0.9-1.1	1	0.5-1.2	1.1
V_{OUT}/V_{CORE}(V)	0.6-1.02	0.5-0.8	0.85	0.45-1.1	0.9
Load Regulation (mV/mA)	<1	0.027	11	10	<1
Total Capacitance (nF)	0.4	0.48	0.14	0.8	23.5
Load Type	Pipelined Core	NA	NMOS	NMOS	Processor
Peak Current Efficiency (%)	97.2	98.4	99	98.3	99.94
Pole position (Bandwidth)	Output node (High)	Internal (Low)	Tri-Loop (Medium)	NA	NA
No of Voltage Domains	2	1	1	1	1
FOM1: Minimum Dropout (mV) at peak V_{IN}	180	300	200	100	200
*FOM2: (Transient Time) * I_{CTL}/I_{MAX} (ns)	4.73	0.32	3.01	76.5	7.75
* Normalized to Technology					

Table 3: LDO comparisons for $V_{DO,MIN}$ and FOMs.

IV. CONCLUSIONS

A digitally-assisted leakage current supply (LCS) circuit lowers the maximum current requirement for analog LDOs to reduce the minimum dropout voltage ($V_{DO,MIN}$), thus expanding the LDO operating range for reducing SoC core power. Silicon measurements from a 130nm test chip demonstrate that the LCS assisted hybrid LDO lowers $V_{DO,MIN}$ by 30-38%, resulting in core power reduction of 21-28% at iso-F_{CLK} within the wider LDO operating range.

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