Switched-Mode-Control Based Hybrid LDO for Fine-Grain Power Management of Digital Load Circuits

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***Abstract*— Switched-mode-control (SMC) is a control methodology that allows instantaneous switching between controllers to extend the dynamic range of feedback circuits. A hybrid low dropout voltage regulator utilizing SMC is designed in 130 nm CMOS for fine-grain power management, fast droop recovery, and accurate voltage regulation of digital load circuits. The design provides an optimal tradeoff between performance and accuracy by switching between a digital and an analog control loop. Measurements from the test-chip show near-threshold-voltage operation, peak transient response of 0.71 ns/mA, and a peak current efficiency of 98.64%.**

***Index Terms*— Adaptive control, digital linear voltage regulators (LVR), embedded power management, low dropout (LDO), low-power digital circuits.**

I. Introduction

FINE-GRAIN point-of-load (PoL) power management on a chip minimizes resistive losses, and enables rapid droop mitigation, high energy-efficiency and fast dynamic voltage, and frequency scaling in multi-core processors and system-on-a-chip designs [1]. Linear voltage regulators mostly operated in the low dropout (LDO) mode are favored PoL regulators due to their small size, process friendly integration, and fast response times [2], [3]. In this paper, we propose a new control topology for LDOs namely, switched-mode-control (SMC) and show its efficacy in designing low-power and fast LDOs covering a wide operational range.

PoL voltage regulation of digital load circuits needs to satisfy a different set of constraints than that offered by traditional analog load circuits [4]. For example, digital circuits can withstand a lower PSR, but require fast transient recovery under large voltage droops and operation down to near-threshold-voltage (NTV) with minimum dropout. To meet these challenges, both analog and digital LDOs are being researched [5]–[12]; and they have their own strengths and weaknesses. Analog LDOs exhibit accurate small signal (SS) regulation, but lack voltage and process scalability and the ability to handle large current transients [5], [6]. On the other hand, digital LDOs are characterized by fast large signal (LS) performance, but they lack high SS gain. They also show steady-state ripple and consume clocking and dynamic power [7]–[11].

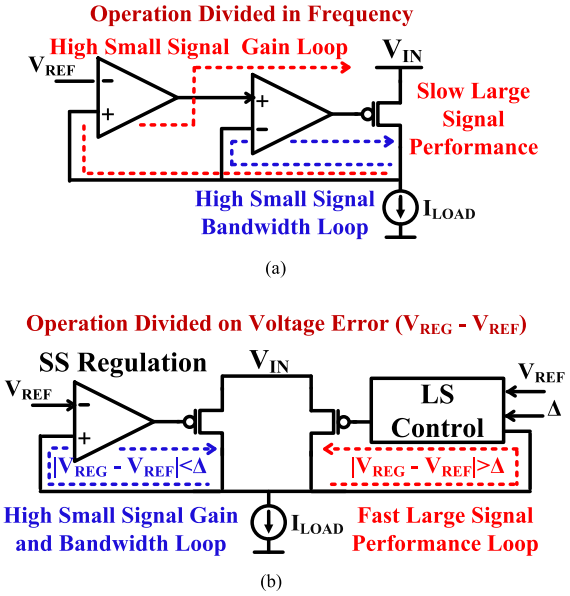

Fig. 1. (a) Conventional dual-loop LDOs. (b) SMC-based multiple controller LDO design.

In this paper, we propose SMC which combines controllers optimized for different metrics to increase operational range and performance without compromising the overall stability. A high-performance SMC-based hybrid LDO designed in a 130 nm CMOS process is presented in this paper. The proposed design decouples the SS gain from LS transient response by utilizing a voltage-based error signal to discretely switch from one controller to another. This is fundamentally different from other dual-loop architectures [5], [12], [13], which employ both the loops simultaneously. In such designs, the bandwidth (BW) of the high-gain loop is decreased to maintain stability [Fig. 1(a)]. The hybrid LDO uses SMC to combine the strengths of both analog and digital LDOs. It combines the LS response (transient performance) of an all-digital loop with the high-gain steady-state voltage regula-

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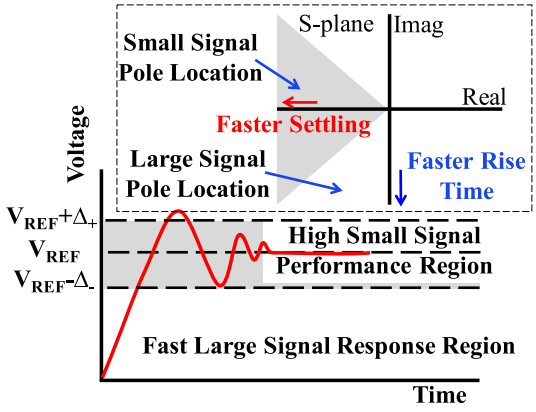


Fig. 2. Ideal closed-loop pole locations for LS and SS controllers.

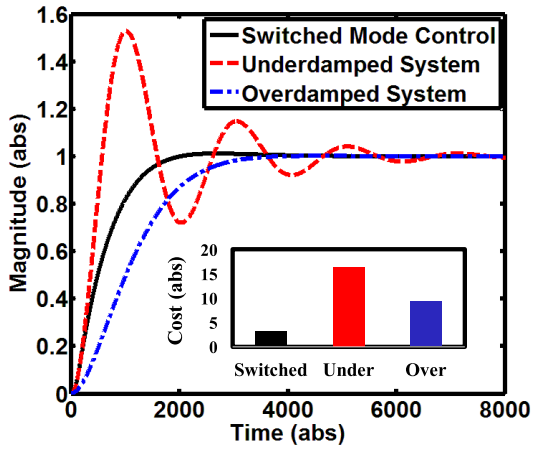


Fig. 3. Effectiveness of SMC compared to a single controller design.

tion offered by an analog loop [see Fig. 1(b)], thus enabling optimal control across a wide operating range. The addition of analog assistance to the digital loop enables a high-performance hybrid LDO operation at higher power supply voltages ranging from 1.2 to 1.1 V. To provide voltage regulation at low power supply voltage down to 0.6 V and still ensure process and design scalability, SMC further enables the hybrid LDO to be turned into an all-digital LDO without compromising design stability or consuming additional power.

The need for using SMC (first presented in [14]) instead of a single controller is motivated in Section II. In Section III, the hybrid LDO architecture is elaborated. Stability modeling of SMC and an ultra-fast response time design feature called SMC with reset control are presented in Sections IV and V, respectively. Circuit implementation of the hybrid LDO is covered in Section VI. Measurement results from the test chip are covered in Section VII followed by conclusions in Section VIII.

II. Motivation for Switched-Mode-Control

Since, digital load circuits exhibit large load current (I_{LOAD}) changes and operate under wide operational voltage ranges (from V_{MAX} to NTV), it is difficult to ensure fast transient response using a single controller across the entire current and voltage range [13]. For example, an analog LDO provides high performance at near-supply input voltage, but

TABLE I

Selection of LS Controller Topology

LS LDO Topology Characterization		
Type of LDO	Analog	Digital
Rise Time	Slow	Fast
Small Signal Gain	High	Low
Process Scalability	Low	High
Design Automation	Low	High
Performance Adaptation	Low	High
Design Choice		✔

TABLE II

Selection of SS Controller Topology

SS Analog LDO Topology Characterization		
Dominant Pole Location	Internal	Output
V_{DROOP}	High	Low
PSR over all frequency	Low	High
UGF	Low	High
Light Load Stability	Poor	Good
On chip Integration	Standard	Difficult
Design Choice		✔

fails at NTV [5] and a digital LDO offers low voltage operation, but shows a reduced power efficiency if operated in high performance mode [4]. Therefore, the motivation for SMC stems from the fact that multiple controllers extend the operational range at a better power efficiency.

The step response of a second order linear system determines all the critical parameters that are needed to ascertain the effectiveness of the feedback. A fast rise time ensures quick recovery from a transient event. A fast and accurate settling ensures accurate tracking of a reference voltage (V_{REF}). On the other hand, a minimum overshoot reduces unwanted ringing. These three factors can be combined into a quantitative cost metric, which characterizes the typical feedback control of an LDO, defined as [15]

$$\text{Cost} = \int_0^\infty t|V_{REF} - V_{REG}|dt. \quad (1)$$

The cost defined earlier, is the minimum integral of time-multiplied absolute-value of error. It shows a high sensitivity to the three discussed parameters crucial to any second-order system dynamics. The cost increases if the rise time is slow or settling takes longer or the response shows large overshoot or undershoot. In linear voltage regulation, optimality criterion for LS region is fast rise time (T_{RISE}). For SS region, it is fast settling time ($T_{SETTLING}$) with minimum overshoot. SMC allows the two separate optimal controllers to be combined by switching at a threshold to achieve an overall optimal response to LS current transients. Location of the dominant pole of the overall system for each controller determines its response, as illustrated in Fig. 2. For a fast LS response, the dominant poles of the system should have a low damping which enables a small T_{RISE}. On the other hand, a short $T_{SETTLING}$ is achieved by placing the dominant poles of the system deep in the left half s-plane. It can be clearly seen

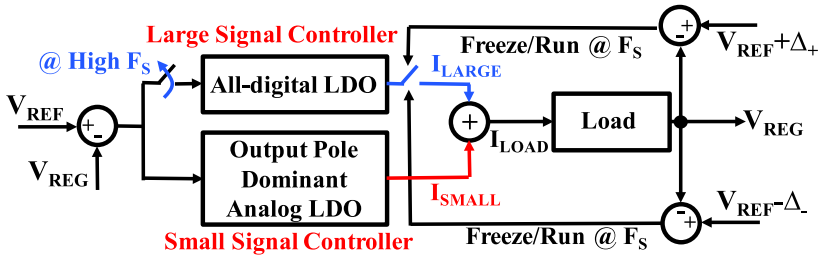


Fig. 4. Control schematic elaborating switching between different controllers based on the voltage error for the proposed hybrid LDO.

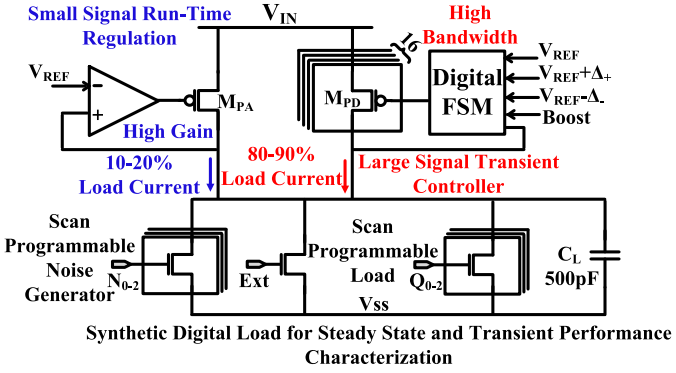


Fig. 5. SMC-based Hybrid LDO architecture with load.

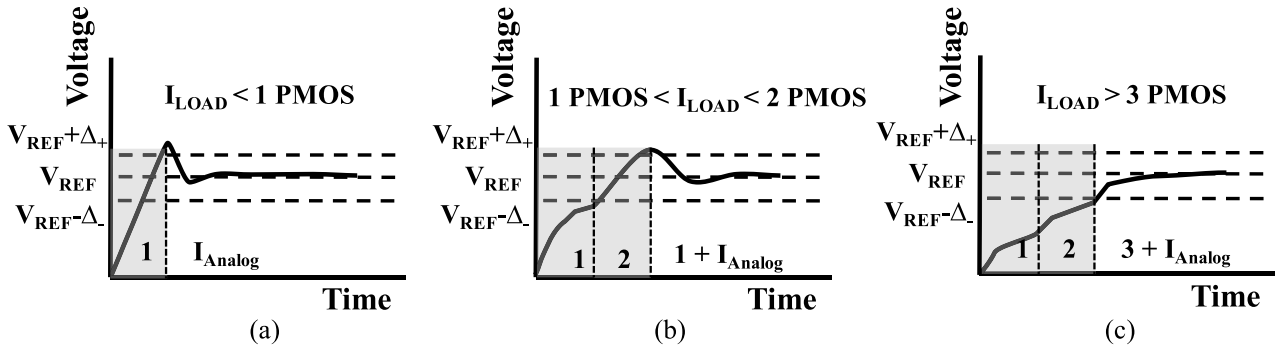


Fig. 6. Operation of hybrid LDO with increasing I_{LOAD}. (a) I_{LOAD} supplied by SS controller only. (b) and (c) I_{LOAD} supplied by both LS and SS controllers (LS clock frequency ∼ output pole frequency).

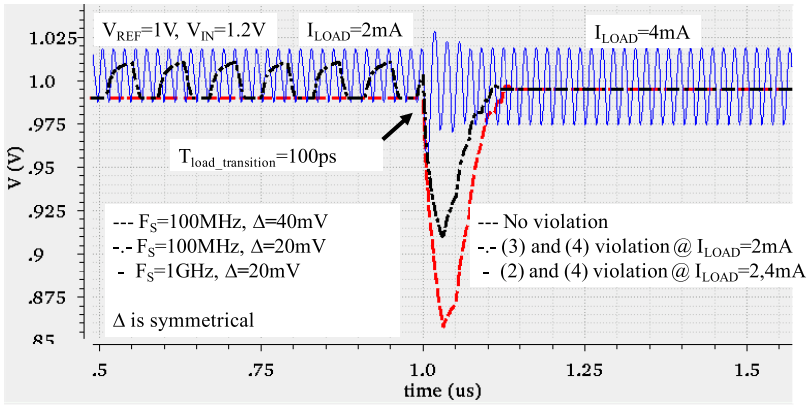


Fig. 7. SPICE simulation of the hybrid LDO showing conditions where stability constraints are violated resulting in an unstable behavior.

that an SMC based on the combination of an underdamped and overdamped controllers outperforms both individually in terms of the cost metric defined in (1) as shown through the step response of different systems in Fig. 3.

A. Use of SMC in Digital LDO Designs

Although we introduce SMC-based LDOs in this paper, it is worth noting that many recent LDO designs with state-of-the-art performance incorporate SMC in one form or the other,

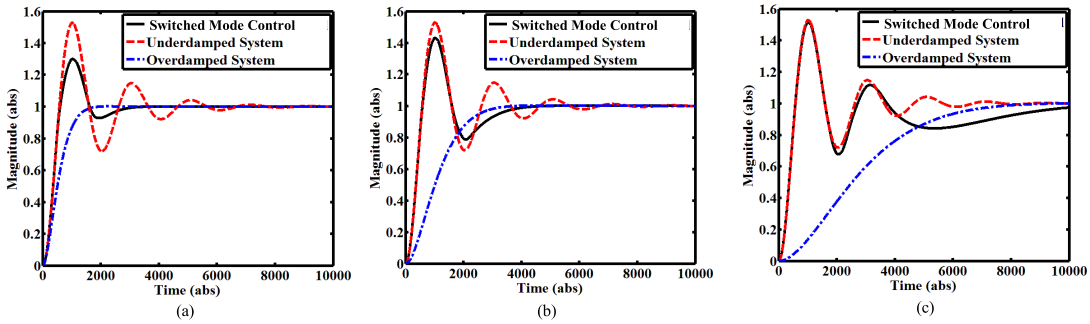


Fig. 8. Decreasing the BW of SS controllers increases the settling time (T_{SETTLING}) of the SMC design. (a) BW(overdamped system) = BW(underdamped system)/3. (b) BW(overdamped system) = BW(underdamped system)/6. (c) BW(overdamped system) = BW(underdamped system)/12.

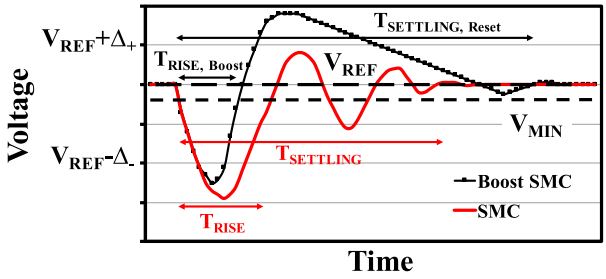


Fig. 9. Reset SMC shows quicker resumption (equal to $T_{\text{RISE,Reset}}$) of digital load circuit operation (the digital load can achieve operational frequency when $V_{\text{REG}} > V_{\text{MIN}}$) after a voltage droop as compared to the SMC (equal to T_{SETTLING}). $V_{\text{REF}} - V_{\text{MIN}}$ = digital load guard-band.

albeit implicitly. Nasir *et al.* [8] and Salem *et al.* [16] have used a single controller but multiple modes of operation (and hence, multiple controllers) to enable fast recovery from load transients. Similarly, Yang *et al.* [9], Huang *et al.* [17], and Tsou *et al.* [18] have used different quantization of power stages to enable fine or coarse-grain control. Multiple controllers in SMC-like configuration are employed in [19] and [20] to achieve fast transient and low ripple steady-state performance. Hence the authors believe that a unifying treatment of SMC is critical to analyze the dynamics of a family of LDOs that have gained popularity. The stability modeling of SMC presented in Section IV can be adapted to model these recently published designs.

III. Hybrid LDO Design Architecture

A. Choice of SS and LS Controllers

Choosing optimal controllers for each region of operation ensures optimal performance across the complete current and voltage operational range. As summarized in Table I, a higher integration density, process scalability, design automation, low voltage operation and most importantly, ultra-fast response without slew limitation, makes digital LDO an ideal choice to act as the LS controller. It allows faster recovery from load transients and offers wider operating voltages. In addition to that, a digital LDO can be adaptively made severely under-damped with a fast clock as desired for the LS controller [8]. For SS controller, a small quiescent power consumption, high SS gain, and ripple-free SS response makes analog LDO the design choice. Analog LDOs can be further divided in to two major categories (Table II), internal pole dominant (IPD) and output pole dominant (OPD) LDOs. OPD analog LDOs offer better PSR, faster droop compensation, and light load stability compared to their IPD counterparts [5]. Therefore, the SS controller design choice should be an OPD analog LDO. It should be mentioned here that a high-resolution digital LDO is ill-suited to be used as an SS regulator as it suffers from LCOs and limited gain unless high dynamic power budget and clock routing resources are available. Conventionally, a small on-die capacitance budget limits its use in PoL voltage regulation as an OPD analog LDO loses its phase margin (PM) with increasing I_{LOAD} for a given output capacitance. The presented hybrid topology overcomes this integration challenge by using LS controller to deliver most of I_{LOAD}, relaxing the constraints on the SS controller design.

B. Hybrid LDO Operation

The digital LS controller turns on a power transistor array in a thermometer fashion until V_{REG} reaches $V_{\text{REF}} - \Delta_-$. Once V_{REG} enters the dead zone, LS controller is clock gated and the SS controller provides the remaining I_{LOAD} bringing V_{REG} to V_{REF}. For an overshoot, $V_{\text{REG}} + \Delta_+$ acts as the dead-zone boundary with SS controller operational when $V_{\text{REG}} < V_{\text{REF}} + \Delta_+$. The LS digital controller power transistors are designed to provide 80%–90% of the I_{LOAD}, whereas the SS analog controller provides the remaining 10%–20% of I_{LOAD} at the maximum current rating. This range is ensured keeping in perspective that an increased I_{LOAD} contribution from the analog LDO diminishes the performance gains of an all-digital LDO as elaborated in [21]. The high operational BW of the LS controller makes SS controller ineffective when it is active and V_{REG} is out of the dead zone. Therefore, there is no need to explicitly turn off the SS controller when $V_{\text{REF}} - V_{\text{REG}} > |\Delta|$. This also helps in eradicating switching noise and power overhead of explicitly switching SS analog controller ON or OFF. The dead zone helps bound the limit cycle oscillations (LCOs) in digital LS controller when it is operated at a high frequency of operation by increasing the stability of the hybrid LDO [4]. The choice of switching thresholds (Δ_- and Δ_+) not only ensures stable operation (no chattering between the two controllers) but also makes sure that the analog LDO only provides a small portion of the total I_{LOAD} (10%–20%), thereby assisting the dominant digital operation of the hybrid LDO through an OPD analog

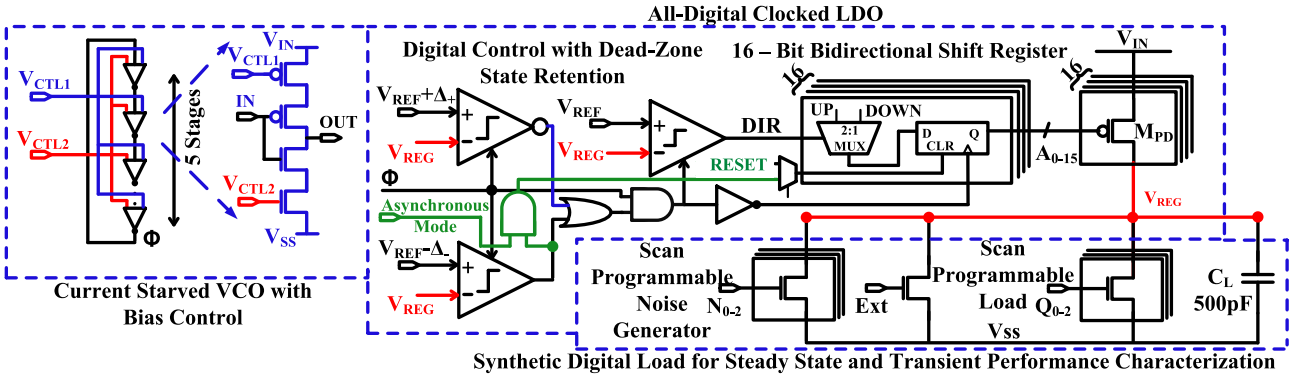


Fig. 10. LS controller with clock generation through a five-stage current-starved VCO. Reset SMC is enabled when Asynchronous mode = 1.

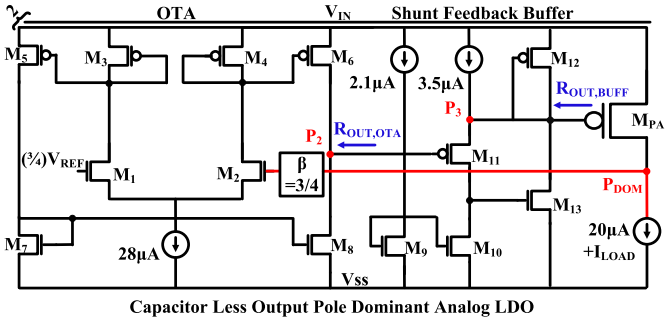


Fig. 11. OPD analog LDO as the SS controller.

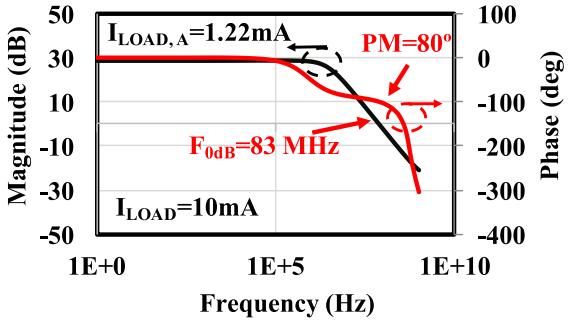


Fig. 12. Simulated PM of the hybrid LDO at $V_{REG} = 1$ V.

LDO design. The switching between the two controllers is summarized through the control schematic, as shown in Fig. 4, and a complete system architecture of the proposed hybrid LDO is shown in Fig. 5 with operational plots in Fig. 6(a)–(c). Digital load circuits are mimicked by NMOS transistors. Their strength is scanning programmable, allowing both transient and steady-state current changes on the order of picosecond. A 500 pF (at 1 V) MOS capacitor serves as the load capacitor to mimic a realistic capacitance offered by a medium-sized digital function unit [10].

IV. Stability Modeling

To stitch a fast and underdamped LS digital controller to a slow and damped SS analog controller in a stable fashion, a dead zone is established using two thresholds above (Δ_+) and below $(\Delta_-)V_{REF}$. The digital LS controller creates LCOs due to its discrete nature of operation. These LCOs are created by periodically turning on/off power transistors. The number of power transistors turned on/off in steady state is called

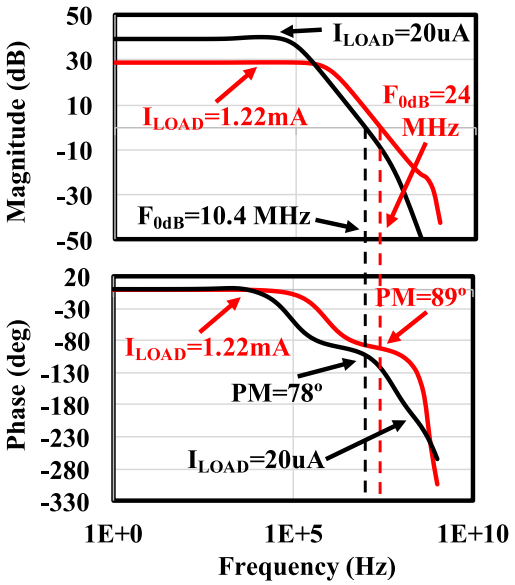
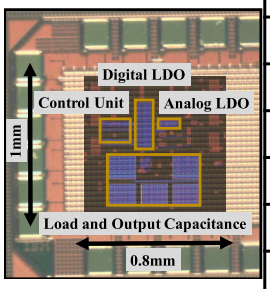


Fig. 13. Simulated PM and unity gain BW of the SS controller across its complete I_{LOAD} range at $V_{REG} = 1$ V.



Process	GF 130nm CMOS
Package	QFN
Active Area	0.0818mm²
V_{IN}	0.6V, 1.1-1.2V
I_{LOAD}	30µA – 12mA
V_{OUT}	0.5-0.55V, 0.8-1.1V
Load Capacitance	< 500 pF

Fig. 14. Die micrograph with chip details.

mode. The mode of LCO increases with higher F_S. As a result, the V_{REG} voltage ripple frequency ($F_{LCO,LS}$) decreases. On the other hand, the V_{REG} voltage ripple amplitude ($A_{LCO,LS}$) decreases when F_S increases, but shows a jump rise whenever the mode of LCO increases. For more details on the existence, conditions, and magnitude of LCO, interested readers are pointed to [4] and [22] for further reading. For stable and chattering-less settling to V_{REF}, the SS controllers

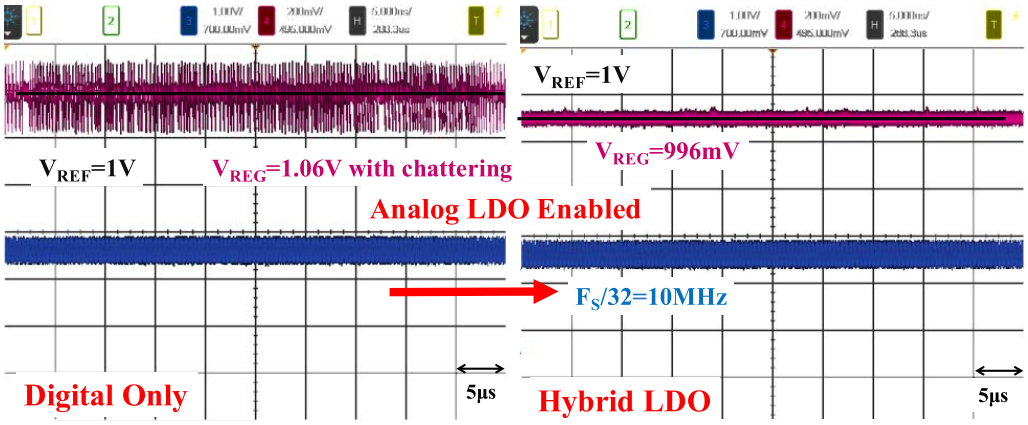


Fig. 15. Scope capture of steady-state response when SS controller is disabled and enabled.

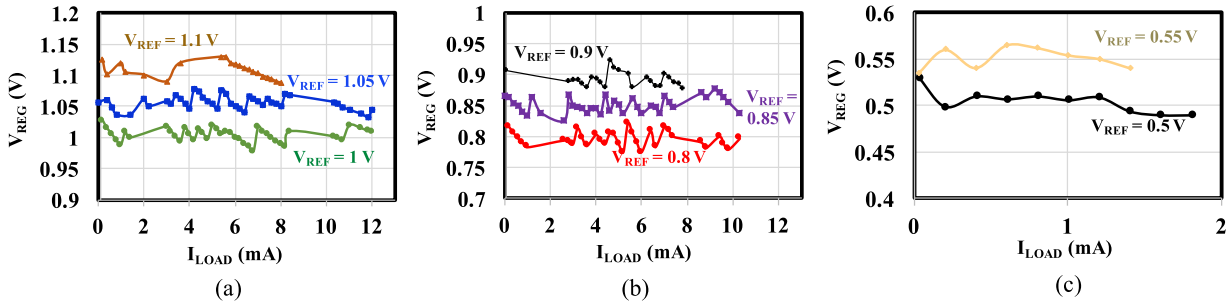


Fig. 16. Load regulation measurements. (a) With $V_{IN} = 1.2$ V (for hybrid). (b) $V_{IN} = 0.6$ V (digital only). Worst case DC error = 32 mV measured at $V_{REF} = 0.8$ V.

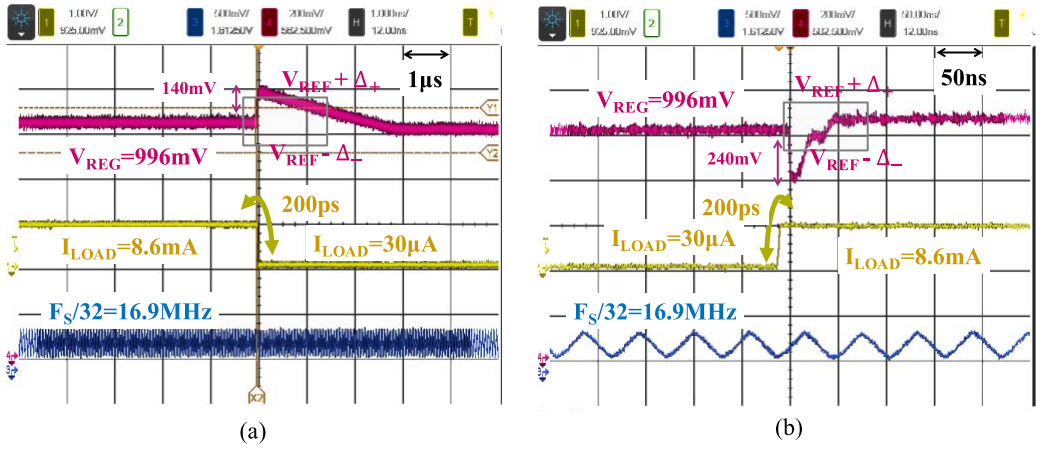


Fig. 17. Scope capture showing hybrid LDO response to (a) I_{LOAD} step down and (b) I_{LOAD} step up.

must have enough loop gain (K_{SS}) and BW ($F_{0\,dB,SS}$) to suppress the oscillations generated the digital LS controller. Stable operation of the hybrid LDO can be achieved by satisfying the design constraints (2)–(4): $A_{LCO,LS}$ and $F_{LCO,LS}$ refer to the voltage ripple amplitude and frequency of the LCO generated by the LS controller if it is operated without any

$$\text{If } A_{LCO,LS} > (V_{REF} + \Delta_+ - V_{REF} + \Delta_-); \quad \text{then} \quad F_{0\,dB,SS} > F_{LCO,LS} \qquad \text{Bandwidth Constraint} \tag{2}$$

$$\text{If } F_{0\,dB,SS} < F_{LCO,LS}; \quad \text{then} \quad A_{LCO,LS} < (V_{REF} + \Delta_+ - V_{REF} + \Delta_-) \qquad \text{Amplitude Constraint} \tag{3}$$

$$V_{REF} - \Delta_- < \left(V_{REF} - \frac{V_{REF}}{1 + K_{SS}}\right) < V_{REF} + \Delta_+ \qquad \text{Small Signal Gain Constraint.} \tag{4}$$

dead-zone and SS controller. The BW constraint in (2), as shown at the bottom of this page, implies that if the dead zone is small compared to the LS controller power transistors quantization then we need $F_{0\,\mathrm{dB,SS}}$ higher than $F_{\mathrm{LCO,LS}}$ to ensure stable settling. On the other hand, the amplitude constraint in (3), as shown at the bottom of this page, implies that if the $F_{0\,\mathrm{dB,SS}}$ is less than $F_{\mathrm{LCO,LS}}$ then $A_{\mathrm{LCO,LS}}$ must be less than the dead zone to ensure stable settling. The SS gain constraint in (4), as shown at the bottom of this page, implies that K_{SS} must be large enough to ensure that the steady-state voltage error is less than the dead-zone size to avoid chattering between LS and SS controllers. One of the BW or amplitude constraints and SS gain constraint must be satisfied to guarantee stable operation of the hybrid LDO. Possible worst case amplitude constraint (3) violations occur under light-load conditions and frequency constraint (2) violations occur at very high operational frequencies as shown in SPICE simulation of Fig. 7.

A large dead zone ensures that multiple power transistors of the LS controllers are needed to traverse it. At iso-F_S, it implies a decreased $F_{\mathrm{LCO,LS}}$ relaxing the specification on $F_{0\,\mathrm{dB,SS}}$. Similarly, a large dead zone also relaxes the specification on K_{SS}. If F_{LCO} induced by the LS controller in the dead zone lies below $F_{0\,\mathrm{dB}}$ of the SS controller, and the dead zone is large to ensure that $A_{\mathrm{LCO,LS}} < (\Delta_+ + \Delta_-)$ then the hybrid LDO is guaranteed to be stable. The exact settling time and accuracy of the output voltage are dependent on the load regulation of the SS controller. A higher $F_{0\,\mathrm{dB}}$ ensures that oscillations in the dead zone quickly die down resulting in faster settling, as shown in Fig. 8. The voltage settles down to V_{REF} within an error bounded by the loop gain (K_{SS}) of the SS regulator.

Although a larger dead-zone enables a more relaxed specification on the BW of the SS controller, it may not be suitable for early detection and mitigation of voltage droops and overshoots. More discussion on the selection of thresholds for the hybrid LDO is carried out in Section VII with test-chip measurements. As evident from the earlier discussion, amplitude and BW conditions for a digital LS controller are easy to formulate owing to its discrete nature of operation. This allows well-posed constraints for achieving stable hybrid LDO operation. In case the LS controller is analog, similar amplitude and frequency conditions can be devised by identifying the natural frequency and damping coefficient from the closed-loop pole location.

V. SMC With Reset Control

Synchronous digital circuits are designed with a guard-band to operate as soon as the voltage is high enough ($\geq V_{\mathrm{MIN}}$, where $V_{\mathrm{MIN}} = V_{\mathrm{REF}}-$ voltage guard-band added to ensure correct operation under variations) to support a target operational frequency (F_{OP}) [23]. Therefore, any voltage higher than V_{MIN} ensures that the underlying circuit can resume operation without any timing errors in the pipeline of digital circuits. For such load circuits, ultra-fast droop recovery to V_{MIN} is necessary for high-performance quick resumption of operation. To meet this requirement, we propose a reset mode

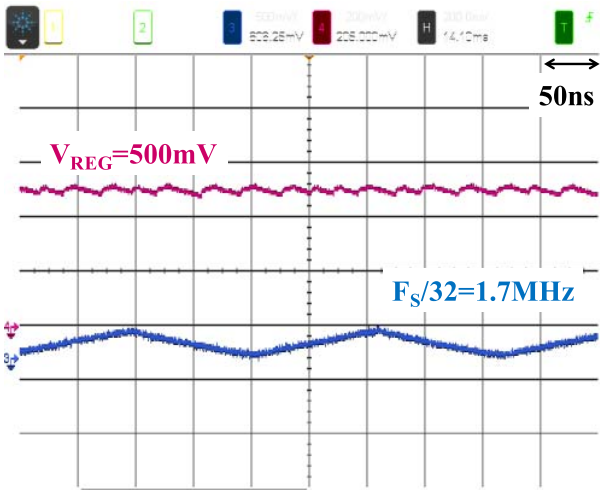


Fig. 18. All-digital LDO configuration with $V_{\mathrm{IN}} = 600$ mV and $V_{\mathrm{REF}} = 500$ mV.

in the hybrid SMC-based LDO. This mode enables ultra-fast droop recovery to V_{REF} under the condition that the constraints on the overshoot are relaxed. In this extreme non-linear design, as soon as the output voltage reaches $V_{\mathrm{REF}} - \Delta_-$, all the power MOSFETs of the digital loop are "turned on," enabling ultra-fast T_{RISE}. After recovering from the droop, the system undergoes a large overshoot (always less than V_{IN} as inherent negative feedback of PMOS V_{SD} kicks in against decreasing voltage headroom) and finally settles down to V_{REF} in an overdamped fashion never falling below V_{MIN}. This reset mode SMC is compared with the regular operation of the hybrid LDO in SMC configuration through the representative operational plot shown in Fig. 9. It shows a faster T_{RISE} ensuring an early resumption of the digital load operation than achievable through the SMC design. This reset mode feature is designed as a part of the digital LS controller. The reset mode is recommended for fast droop recovery under large transient events like clock un-gating and under the assumption that the constraints on the overshoot are relaxed. The reset mode is enabled by the non-linear SMC by allowing the loop dynamics to be completely different in the two regions: quick and underdamped in undershoot and slow and overdamped in overshoot.

VI. Hybrid LDO Circuit Implementation

A. LS Controller Design

A synchronous all-digital LDO with 16 output power transistors is implemented. The small array size with large power transistors as opposed to a larger array size with smaller transistors guarantees a fast LS response [8]. It comprises of four stages, namely, a detection stage to determine the magnitude of the voltage error, a comparison stage to determine the sign of the voltage error, a control stage, and an actuator stage. The detection stage consists of two strongARM latch-based clocked comparators. They are used to compare V_{REG} with $V_{\mathrm{REF}} - \Delta_-$ and $V_{\mathrm{REF}} + \Delta_+$ to establish if V_{REF}–$V_{\mathrm{REG}} > |\Delta|$. The comparators are designed to operate up to 1 GHz. If V_{REG} is found to be $< V_{\mathrm{REF}} - \Delta_-$ or $> V_{\mathrm{REF}} + \Delta_+$, i.e., out of the dead zone, the clock signal is un-gated to the

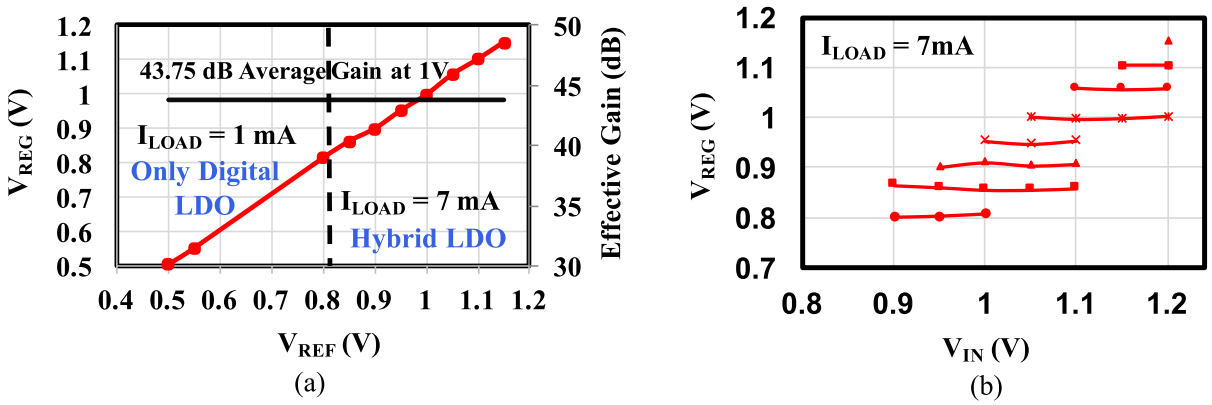


Fig. 19. Line regulation measurements with (a) $V_{IN} = 1.2$ V (for hybrid) and $V_{IN} = 0.6$ V (digital only) and (b) with complete V_{IN} range for hybrid LDO.

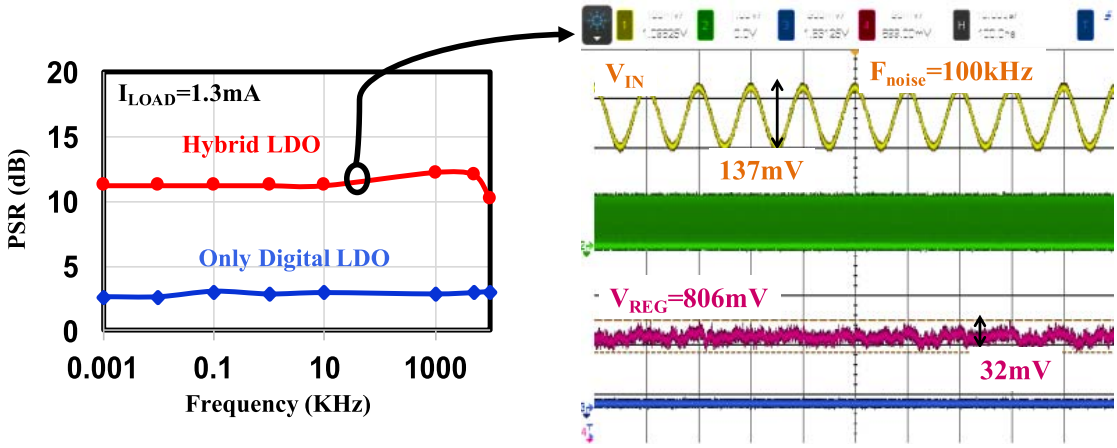


Fig. 20. PSR measurements with $V_{IN} = 1.2$ V (for hybrid), $V_{IN} = 0.6$ V (digital only) with a scope capture when $F_{NOISE} = 100$ kHz.

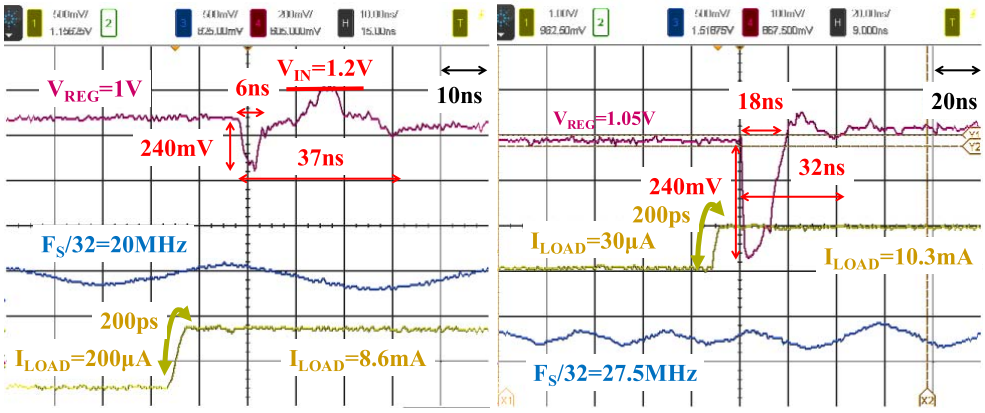


Fig. 21. Measured operation and droop recovery for (a) reset mode SMC and (b) SMC.

following comparison stage. The comparison stage consists of a single strongARM latch-based clocked comparator. It is only operational if the clock is available to it from the preceding detection stage. Once ON, it compares V_{REG} with V_{REF}. The control stage consists of a 16-bit bidirectional shift register. If $V_{REG} < V_{REF}$, the shift register passes a "0" to turn on a power transistor and if $V_{REG} > V_{REF}$ then it passes a "1" to turn off a power transistor, in the final actuator stage. The comparison stage operates at the positive clock edge, whereas, the control stages uses the negative clock edge for its operation. This dual edge triggering allows a lower control signal latency. The final actuator stage consists of an array of 16 power transistors.

In reset mode, all the transistors are instantaneously switched ON by resetting the shift register when a droop is detected by $V_{REF} - \Delta_-$ comparator. A regular digital LDO

operation is resumed for $V_{\mathrm{REG}} > V_{\mathrm{REF}}$ at a slower F_S. The power transistor array is designed to provide a maximum current (I_{LOAD}) of 12 mA consuming a total area of 27.68 μm^2. The clock for the LS controller is generated with five-stage current-starved inverter-based voltage controlled oscillator (VCO). The bias voltage control of this VCO is available externally on a pad. The oscillator frequency can be tuned up to 1 GHz. A detailed circuit implementation of the LS controller along with the current-starved VCO is shown in Fig. 10.

B. SS Controller Design

An OPD analog LDO is designed to provide high gain and BW for SS regulation. The proposed LDO is designed to deliver 40 μA to 2.5 mA without the use of any internal capacitors to achieve stable operation. This is achieved by creating two replicas, each capable of providing up to 1.25 mA current while consuming less than 82 μA quiescent current combined. The first stage of the OPD analog LDO comprises of a self-biased transconductance (g_m) stage. It uses a differential pair with diode-connected load transistors, as shown in Fig. 11. To make the output node pole dominant, all the internal poles of the LDO need to be at frequencies at least 10× higher than the output pole. This is achieved by employing two separate techniques as follows.

1) Using smaller size of the power transistor through the hybrid topology.
2) Putting in a shunt buffer between the first stage and the power transistor to further push the pole at the gate of the power transistor to a higher frequency

An adaptive shunt buffer stage is inserted between the power transistor and the g_m stage [24]. If the first stage is directly connected to the power transistor, the impedance at the power transistor gate is not small enough to guarantee the stability with the output capacitance in a sub-nanofarad range. Therefore, the shunt buffer stage is used to divide this pole (second dominant) into two high-frequency poles calculated as

$$P_2 \approx 1/2\pi\, R_{\mathrm{OUT,OTA}} C_{\mathrm{GS},M11} \tag{5}$$

$$P_3 \approx 1/2\pi\, R_{\mathrm{OUT,BUFF}} C_{\mathrm{GS,MPA}} \approx \mathrm{gm}_{11}(1+\mathrm{gm}_{13})+\mathrm{gm}_{12})/2\pi\, C_{\mathrm{GS,MPA}}. \tag{6}$$

P_2 is pushed to a higher frequency, as the gate capacitance offered by M_{11} is very small compared to that of M_{PA}. P_3 is pushed to a higher frequency as the resistance at the gate of M_{PA} decreases due to the shunt feedback implemented through transistors M_{11}–M_{13}. M_{11} samples the voltage at the gate of the power MOS and uses M_{13} to adjust the current to complete the shunt feedback loop.

Worst stability condition for the SS regulator occurs at the maximum I_{LOAD}, as the dominant output pole is at its highest possible frequency. Maintaining a high PM requires the shunt feedback loop to be effective when the voltage at the gate of M_{PA} has decreased to provide maximum I_{LOAD}. This is ensured by increasing the biasing current flowing through the diode-connected transistor M_{12} through the increased V_{GS}.

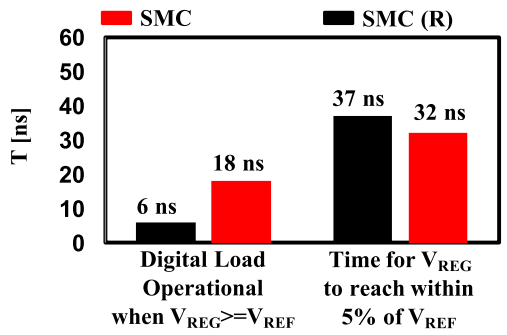


Fig. 22. Measurements show that a faster T_{RISE} for reset SMC enables quicker resumption of operation of digital load after a droop as compared to the SMC (Digital load is assumed to operate when $V_{\mathrm{REG}} > V_{\mathrm{REF}}$). On the other hand, SMC shows faster T_{SETTLING} as compared to the reset SMC.

A simulated bode plot near I_{MAX}, as shown in Fig. 12, highlights the achieved high PM at a high I_{LOAD} condition.

C. Stability Analysis of the Hybrid LDO

As mentioned in Section III, SS controller is designed to reject the noise in the dead zone created by the LS controller. SS load regulation capacity of the SS controller is equivalent to its loop gain and BW. Given the adaptive nature of the shunt feedback buffer, P_3 is the least dominant pole that adapts with changing I_{LOAD}. Therefore, loading at output of the buffer can be neglected resulting in a second-order SS loop gain for the SS controller given as

$$\text{Loop Gain}(s) \approx \frac{-0.75\mathrm{gm}_{\mathrm{OUT,OTA}} R_{\mathrm{OUT,OTA}} \mathrm{gm}_{\mathrm{MPA}} R_{\mathrm{LOAD}}}{(1+sR_{\mathrm{OUT,OTA}}C_{\mathrm{GS},M11})(1+sR_{\mathrm{LOAD}}C_{\mathrm{LOAD}}).} \tag{7}$$

The location of the P_{DOM} is directly proportional to the I_{LOAD} given as

$$P_{\mathrm{DOM}} \approx I_{\mathrm{LOAD}}/2\pi\, V_{\mathrm{LOAD}} C_{\mathrm{LOAD}}. \tag{8}$$

As evident from the bode plot in Figs. 12 and 13, the system behaves like a single pole system in the specified current range. The unity gain BW ($F_{0\,\mathrm{dB,SS}}$) of the SS regulator across I_{LOAD} is 10.4 ($I_{\mathrm{LOAD}} = 20$ μA) and 84 MHz ($I_{\mathrm{LOAD}} = 10$ mA), and the loop gain (K_{SS}) ranges from 40 ($I_{\mathrm{LOAD}} = 10$ mA) to 28 dB ($I_{\mathrm{LOAD}} = 20$ μA).

On the other hand, the LS controller induces $F_{\mathrm{LCO,LS}} = 46$ MHz and $A_{\mathrm{LCO,LS}} = 66$ mV at $I_{\mathrm{LOAD}} = 10$ mA and $F_S = 1$ GHz and $F_{\mathrm{LCO,LS}} = 63$ MHz and $A_{\mathrm{LCO,LS}} = 254$ mV at $I_{\mathrm{LOAD}} = 2$ mA and $F_S = 1$ GHz for dropout voltage of 200 mV. These results are obtained through simulations when LS controller is enabled without any dead zone with a dropout of 200 mV. We observe that at $I_{\mathrm{LOAD}} = 10$ mA, $F_{0\,\mathrm{dB,SS}} > F_{\mathrm{LCO,LS}}$ satisfying (2) and at $I_{\mathrm{LOAD}} = 2$ mA ($I_{\mathrm{LOAD}} >$ single digital power transistor), $A_{\mathrm{LCO,LS}} <$ | dead zone | satisfying (3). Throughout these operating conditions, I_{BIAS} of analog SS controller ensures that (4) is always satisfied. In case, $I_{\mathrm{LOAD}} < 2$ mA ($I_{\mathrm{LOAD}} <$ single digital power transistor), and $F_S = 1$ GHz, $A_{\mathrm{LCO,LS}}$ is less than 5 mV due to the low-pass filtering effect of the high operational frequency of the digital LS controller [4]. As a result, (3) is always satisfied resulting in stable operation of

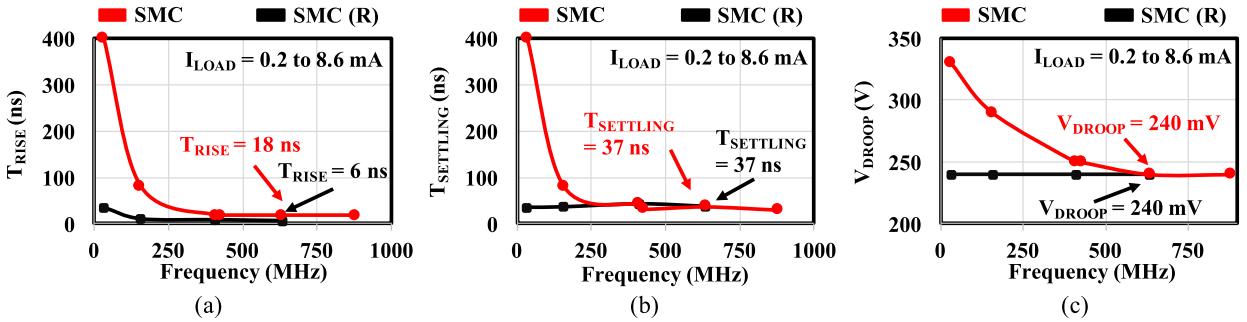


Fig. 23. Measurements showing a comparison between boost SMC and SMC for (a) T_{RISE} (b) T_{SETTLING}, and (c) V_{DROOP} with increasing F_S of the digital LS controller.

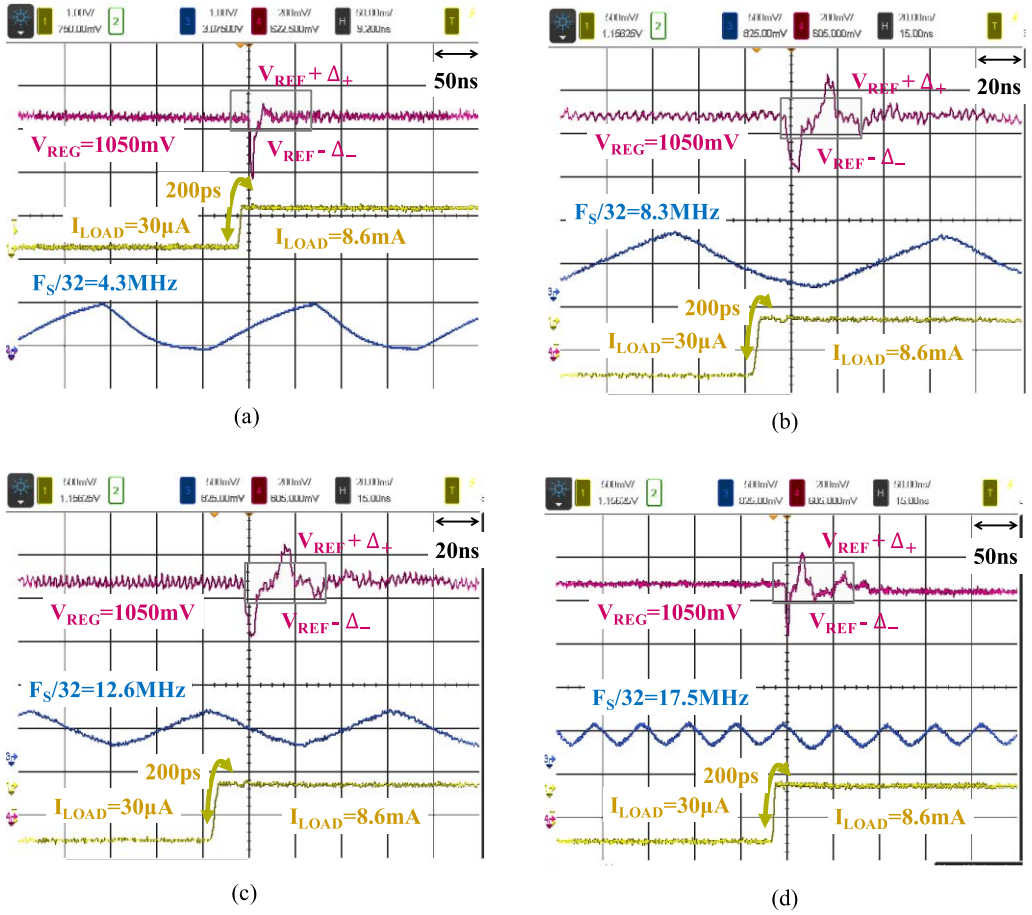


Fig. 24. (a)–(d) Scope captures show that a higher F_S increases the V_{REG} excursions to the dead-zone thresholds, but the gain and BW of the SS controller ensures that the system settles down accurately.

the hybrid LDO even under light-load conditions (bounded by the minimum I_{LOAD} for stable operation of the SS analog controller). Thanks to the adaptive $F_{0\,\mathrm{dB,SS}}$ of the SS regulator due to its OPD configuration, stability constraints of SMC defined in Section IV are always satisfied resulting in a stable operation of the proposed hybrid LDO across the complete operational range.

VII. Measurement Results

Chip micrograph of the presented hybrid LDO fabricated in 130 nm CMOS is shown in Fig. 14. The LDO runs from a V_{IN} of 1.1 to 1.2 V with a dropout (V_{DO}) = 100–300 mV and provides I_{LOAD} = 12 mA at a nominal V_{DO} = 100 mV. For V_{IN} = 0.6 V (NTV mode), the LDO is reconfigured to operate in a fully digital mode. It regulates for a minimum of V_{DO} = 50 mV and provides up to I_{LOAD} = 2 mA at V_{REG} = 0.5 V. Chattering (unstable behavior) is observed when the analog SS controller is turned off and shows accurate steady-state settling once it is enabled, as shown in the scope captures of Fig. 15. Extensive load regulation measurements (Fig. 16) are performed across the complete operational range including hybrid and all-digital modes. The worst case measurement

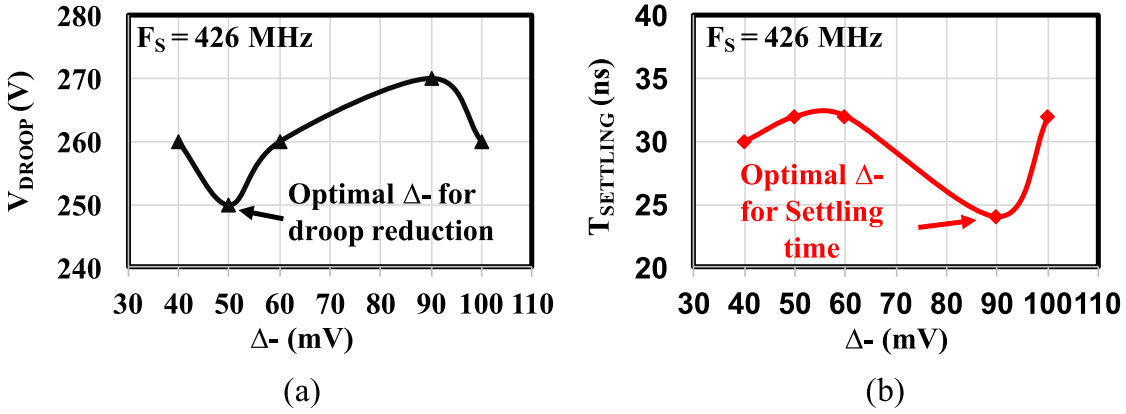


Fig. 25. Measurements for selection of optimal Δ_- for (a) droop reduction and (b) settling time.

showed 2.67 mV/mA for I_{LOAD} up to 12 mA and 3.1 mV/mA for the maximum transient load step change of 10.3 mA. Load regulation can be further improved by increasing the SS controller gain at maximum I_{LOAD}. A T_{RISE} and T_{SETTLING} of 25 and 45 ns are measured for a load step from 30 μA to 8.6 mA and a T_{SETTLING} of 2.8 μs is measured from an overshoot generated for a load step from 8.6 mA to 30 μA as captured on scope in Fig. 17. In this case, LS controller is operated at an $F_S = 540$ MHz. The hybrid LDO is turned into an all-digital LDO for $V_{\text{IN}} <= 600$ mV operating at 54.4 MHz. Scope capture proves regulation at $V_{\text{REF}} = 500$ mV with a small ripple as shown in Fig. 18.

The hybrid topology exhibits high line regulation (on average $<$ 5 mV error), as shown by the linearity of graph in Fig. 19. A 43.75 dB average gain is measured at 1 V from the measurements for the complete operational range of the hybrid LDO. As opposed to purely digital LDO topologies, which fail to provide considerable power supply noise rejection (PSR), the presented hybrid topology shows an average of 10–12 dB PSR from 1 Hz to 10 MHz. As shown in Fig. 20, the high BW of the PSR graph (and the absence of PSR peaking which is typical of IPD LDOs due to degradation of the loop gain) also demonstrates the OPD behavior of the designed SS controller. Scope capture shows a PSR greater than 9 dB at 100 kHz (see Fig. 20). The improved PSR in the hybrid topology stems from the noise rejection capability of the analog SS controller. This is in stark contrast to an all-digital controller where we measured a nominal PSR of only 3 dB.

Fig. 21 shows the scope capture of fast transient response both in SMC and reset SMC modes. A $T_{\text{RISE}} = 18$ ns and $T_{\text{SETTLING}} = 32$ ns ($<$2% of V_{REG}) are achieved for a load step of 30 μA to 10.3 mA at $V_{\text{REG}} = 1.05$ V from $V_{\text{IN}} = 1.2$ V in the SMC mode. In the reset mode, a $T_{\text{RISE}} = 6$ ns and $T_{\text{SETTLING}} = 37$ ns ($<$2% of V_{REG}) are achieved for a load step of 200 μA to 8.6 mA (200 ps rise/fall time) at $V_{\text{REG}} = 1.05$ V from $V_{\text{IN}} = 1.2$ V. In comparison, a digital load circuit that operates for $V_{\text{REG}} \geq V_{\text{REF}}$ can resume operation after just 6 ns in reset mode as compared to 18 ns in SMC mode, as summarized in Fig. 22. This represents a droop recovery time of 0.71 ns/mA compared to 1.74 ns/mA, for

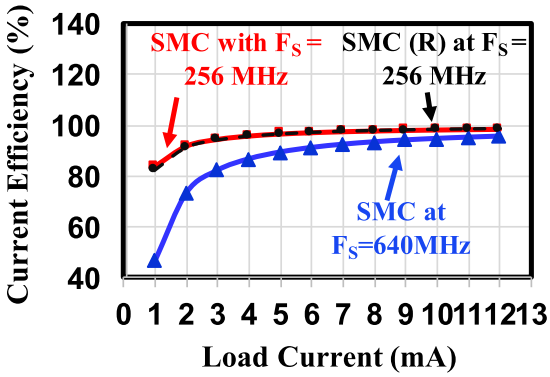


Fig. 26. Measured current efficiency of the hybrid LDO.

SMC-based design. Reset mode SMC provides the best response in droop mitigation and rise time. Measurements show that SMC achieves a comparable performance to the reset mode with increasing F_S of the LS controller. In terms of settling time for V_{REG}, SMC becomes faster than the reset mode SMC as F_S of the LS controller increases (see Fig. 23). This can be easily explained by the fact that the reset mode SMC design overcompensates the voltage droop and discharges slowly to V_{REF}. The slow discharge, however, ensures stable and smooth settling in the reset mode. A worst case voltage droop of 240 mV is measured in both reset and nominal mode at high F_S ($>$ 600 MHz). The large voltage droop magnitude is attributed to the clocked comparator sampling delay, 200 ps step transition in load conditions and small on-chip MOS decoupling capacitor of 500 pf.

As elaborated in Sections III and IV, in SMC, we can employ a higher LS controller F_S and use adaptive BW of SS controller and dead zone to ensure that the hybrid LDO is stable. Scope captures for increasing LS controller F_S shows that V_{REG} does not undergo any oscillation between the two thresholds when $F_S \approx 138$ MHz; whereas, it undergoes only a single oscillation between the two thresholds before it settles down even at a higher $F_S \approx 560$ MHz. In all the scope captures of Fig. 24, stable settling of $V_{\text{REG}} = V_{\text{REF}}$ can be observed. As discussed in Section IV, an optimal placement of the two

TABLE III
COMPARISON WITH STATE-OF-THE-ART

	This Work	[12]	[5]	[8]	[9]	[19]	[16]
Type	LDO	LDO	LDO	LDO	LDO	LDO	LDO
Technology	130 nm	45 nm SOI	65 nm	130 nm	65 nm	28nm	65nm
LDO Type	Digital + Analog	Multiloop	Analog	Digital	Digital	Digital	Digital
Control methodology	SMC	Linear	Linear	Adaptive	Linear	SMC like	SMC like
Control Reconfigurability	Yes	No	No	Yes	No	No	No
VIN (V)	0.6, 1.1-1.2	1.179 - 1.625	1.15	0.5 - 1.2	0.6 - 1.0	1.1	0.45-1
VOUT (V)	0.5 - 0.55, 0.8 - 1.1	0.9 - 1.1	1	0.45 - 1.14	0.55 - 0.95	0.9	0.4-0.95
Load Current: IMAX (mA)	12	42	10	4.6	500	200	0.014-3.3
Load Regulation (mV/mA)	< 2.67 @ 1V	9.8	0.15 - 0.2	< 10	0.25	NA	NA
Controller Current: ICTL(uA)	163.2	9450	50	24 - 221	300	110	8.1-258
Total Capacitance (nF)	0.5	1.46	0.14	1	1.5	23.5	100
Active Area (mm^2)	0.0818	0.075	0.0234	0.114	0.158	0.021	0.03
Peak Current Efficiency (%)	98.5 (R), 98.64 (Linear)	77.50	99.50	98.30	99.99	99.94	99.20
Droop (mV) @ Load Step (mA)	240 @ 10.3 (R)	7.6 @ 4.5	43 @ 10	40 @ 0.7	35 @ 100	120@180	34 @ 1.44
Droop recovery time (ns)	6 (R), 18 (Linear)	NA	100	300	40	NA	11200
FOM1 (ns/mA)	0.58 (R), 1.747 (Linear)	NA	10	428.5	0.4	NA	NA
FOM2 (ps)	166 (R), 244.8 (Linear)	62.4	3.01	0.0765*	1.6	7.75	20

FOM1= Droop recovery time / Load Step; FOM2= (Transient Time) * ICTL/ IMAX
NA - Insufficient data; * Normalized to technology node

thresholds helps achieve a near-optimal damped response to transient I_{LOAD} changes. Measurements from the test chip illustrate this and are shown in Fig. 25. For early detection and minimization of droop, we need a $V_{\mathrm{REF}} - \Delta_-$ closer to V_{REF} ($\Delta_- = 50$ mV). This in turn causes larger overshoots resulting in longer T_{SETTLING}. We observe minimum T_{SETTLING} when $\Delta_- = 90$ mV. When this lower threshold is further decreased, a higher contribution from the SS regulator results in a slower response. The measurements in this paper are made for $\Delta_- = 90$ mV. The system shows a damped response after undergoing an overshoot, therefore, $\Delta_+ = 25$ mV is selected for stable response. A peak current efficiency of 98.64% is measured at $I_{\mathrm{LOAD}} = 12$ mA and $F_S = 256$ MHz. The current efficiency curves across the complete I_{LOAD} range are shown in Fig. 26. These measurements include all the dynamic power consumed in clock generation and distribution. Techniques like bias programming during power saving modes can be used to further improve the current efficiency of analog SS regulator. Competitive performance is achieved in transient response times and operational voltage range when compared with state-of-the-art, as summarized in Table III.

VIII. CONCLUSION

A hybrid LDO based on SMC designed in 130 nm CMOS process featuring both digital and analog loops is presented in this paper. It utilizes SMC as a control law that allows a wider dynamic range of operation both in voltage and current. Stability and performance modeling of SMC are presented in detail and can be applied to related designs as elaborated in the paper. The hybrid LDO design is tailored to meet PoL voltage regulation in digital load circuits with wide workload dynamics. Measurements from the test chip show NTV operation, fast transient response of 0.71 ns/mA, and a peak current efficiency of 98.64%.

REFERENCES

[1] Z. Toprak-Deniz *et al.*, "Distributed system of digitally controlled microregulators enabling per-core DVFS for the POWER8 microprocessor," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2014, pp. 98–99.

[2] T. Singh *et al.*, "Zen: A next-generation high-performance ×86 core," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 52–53.

[3] V. Krishnaswamy *et al.*, "Fine-grained adaptive power management of the SPARC M7 processor," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2015, pp. 1–3.

[4] S. B. Nasir, S. Gangopadhyay, and A. Raychowdhury, "All-digital low-dropout regulator with adaptive control and reduced dynamic stability for digital load circuits," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8293–8302, Dec. 2016.

[5] Y. Lu, W.-H. Ki, and C. P. Yue, "A 0.65 ns-response-time 3.01 ps FOM fully-integrated low-dropout regulator with full-spectrum power-supply-rejection for wideband communication systems," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2014, pp. 306–307.

[6] W.-C. Chen, Y.-P. Su, Y.-H. Lee, C.-L. Wey, and K.-H. Chen, "0.65 V-input-voltage 0.6 V-output-voltage 30 ppm/°C low-dropout regulator with embedded voltage reference for low-power biomedical systems," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2014, pp. 304–305.

[7] Y. Okuma *et al.*, "0.5-V input digital LDO with 98.7% current efficiency and 2.7-μA quiescent current in 65 nm CMOS," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2010, pp. 1–4.

[8] S. B. Nasir, S. Gangopadhyay, and A. Raychowdhury, "A 0.13 μm fully digital low-dropout regulator with adaptive control and reduced dynamic stability for ultra-wide dynamic range," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2015, pp. 1–3.

[9] F. Yang and P. K. T. Mok, "A 0.6–1 V input capacitor-less asynchronous digital LDO with fast transient response achieving 9.5 b over 500 mA loading range in 65-nm CMOS," in *Proc. 41st Eur. Solid-State Circuits Conf. (ESSCIRC)*, 2015, pp. 180–183.

[10] S. Gangopadhyay, D. Somasekhar, J. W. Tschanz, and A. Raychowdhury, "A 32 nm embedded, fully-digital, phase-locked low dropout regulator for fine grained power management in digital circuits," *IEEE J. Solid-State Circuits*, vol. 49, no. 11, pp. 2684–2693, Nov. 2014.

[11] C.-C. Chiu *et al.*, "A 0.6 V resistance-locked loop embedded digital low dropout regulator in 40 nm CMOS with 77% power supply rejection improvement," in *Proc. Symp. VLSI Circuits*, 2013, pp. C166–C167.

[12] J. F. Bulzacchelli, "Dual-loop system of distributed microregulators with high DC accuracy, load response time below 500 ps, and 85-mV dropout voltage," *IEEE J. Solid-State Circuits*, vol. 47, no. 4, pp. 863–874, Apr. 2012.

[13] P. Hazucha, T. Karnik, B. A. Bloechel, C. Parsons, D. Finan, and S. Borkar, "Area-efficient linear regulator with ultra-fast load regulation," *IEEE J. Solid-State Circuits*, vol. 40, no. 4, pp. 933–940, Apr. 2005.
[14] S. B. Nasir, S. Sen, and A. Raychowdhury, "A 130 nm hybrid low dropout regulator based on switched mode control for digital load circuits," in *Proc. 42nd Eur. Solid-State Circuits Conf. (ESSCIRC)*, 2016, pp. 317–320.
[15] D. Graham and R. C. Lathrop, "The synthesis of 'optimum' transient response: Criteria and standard forms," *Trans. Amer. Inst. Elect. Eng. II, Appl. Ind.*, vol. 72, no. 5, pp. 273–288, Nov. 1953.
[16] L. G. Salem, J. Warchall, and P. P. Mercier, "A 100 nA-to-2 mA successive-approximation digital LDO with PD compensation and sub-LSB duty control achieving a 15.1 ns response time at 0.5 V," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 340–341.
[17] M. Huang, Y. Lu, S.-P. U., and R. P. Martins, "An output-capacitor-free analog-assisted digital low-dropout regulator with tri-loop control," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 342–343.
[18] W.-J. Tsou *et al.*, "Digital low-dropout regulator with anti PVT-variation technique for dynamic voltage scaling and adaptive voltage scaling multicore processor," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 338–339.
[19] Y.-J. Lee *et al.*, "A 200 mA digital low-drop-out regulator with coarse-fine dual loop in mobile application processors," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Jan./Feb. 2016, pp. 150–151.
[20] D. Kim, J. Kim, H. Ham, and M. Seok, "A 0.5 V-VIN 1.44 mA-class event-driven digital LDO with a fully integrated 100 pF output capacitor," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 346–347.
[21] S. B. Nasir and A. Raychowdhury, "Embedded hybrid LDO topologies for digital load circuits," in *Proc. IEEE Asia Pacific Conf. Circuits Syst. (APCCAS)*, Oct. 2016, pp. 43–46.
[22] S. B. Nasir and A. Raychowdhury, "On limit cycle oscillations in discrete-time digital linear regulators," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2015, pp. 371–376.
[23] C. Tokunaga *et al.*, "A graphics execution core in 22 nm CMOS featuring adaptive clocking, selective boosting and state-retentive sleep," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2014, pp. 108–109.
[24] M. Al-Shyoukh, H. Lee, and R. Perez, "A transient-enhanced low-quiescent current low-dropout regulator with buffer impedance attenuation," *IEEE J. Solid-State Circuits*, vol. 42, no. 8, pp. 1732–1742, Aug. 2007.

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