A 65nm, 1.15-0.15V, 99.99% Current-efficient Digital Low Dropout Regulator with Asynchronous Non-linear Control for Droop Mitigation

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***Abstract*—Digital LDOs enable on-chip fine-grain power management in multi-core microprocessor and system-on-a-chip platforms to increase system level energy efficiency. Their design synthesizability with automatic placement and routing can enable per-core DVFS with quick design turnaround. To enable per-core voltage regulation, this paper showcases a digital LDO designed in 65nm CMOS process. The LDO exhibits core-level high load current driving capability of up to 125mA and a large voltage regulation range of 0.15V to 1.15V. The design employs asynchronous nonlinear control to achieve fast voltage droop mitigation under large load transient events. Measurements show a peak current efficiency of 99.9% and greater than 99.5% at a light load of only 4mA and 1nF load decoupling capacitance.**

I. Introduction

Digital low dropout (LDO) voltage regulator has emerged as a suitable candidate for on-chip voltage conversion and regulation of digital load circuits [1]. The prime motivation for employing digital LDOs stem from the fact that they can enable on-chip fine-grain power management. Thanks to their digital logic synthesizability and automated placement and routing, they can enable per-core DVFS in large microprocessors and systems-on-chip (SoC) at a low design complexity and integration time. To serve this end, this paper showcases a digital LDO with load current driving capability of up to 125mA enabling per-core voltage regulation. The design allows maximum digital process flow synthesizability, fast asynchronous sensing for transient events and uses nonlinear control to achieve fast voltage droop mitigation.

The trade-offs on voltage regulation metrics offered by a digital LDO are different from that of an analog LDO. These metrics are tailored for powering digital circuits that have large operational ranges (voltage and current) and undergo sudden transitions. A digital LDO allows very low supply voltage operation and high current density. Low supply voltage operation is achieved through digital logic and absence of any biasing requirements. A higher current density is achieved as the power transistors in digital LDO are completely turned on or off in contrast to an analog LDO, where the power transistor is maintained in weak inversion or saturation. Complete on/off switching of power transistors further results in higher voltage droop reduction and faster recovery due to sudden load current transients. On the downside, a digital LDO has low small-signal gain under limited power budget for operational clock generation and distribution. As a result, metrics relevant to noise-sensitive analog load circuits like voltage ripple and power supply noise rejection are inherently low [2].

In its basic form, a digital LDO discretizes both control and power stage by using clock for synchronous sensing and on/off switching of small power transistors instead of a single large power transistor [3]. This quantized nature results in an inherent trade-off between the transient and steady-state performance of a digital LDO [4]. A faster sampling clock can improve transient performance against sudden load changes but during steady-state it results in an increased voltage ripple due to limit cycle oscillations [5]. To decouple steady-state response from transient performance, this paper proposes to asynchronously sense load transients to differentiate it from steady-state operation. This obviates the need for employing a fast clock to meet a transient specification significantly saving power otherwise, expanded in fast clock generation and distribution. Secondly, to enable ultra-fast voltage droop recovery, we employ non-linear control which results in maximum droop mitigation against large load transients under limited decoupling capacitance budget. This topology is especially suitable for load circuits that can remain operational when regulated voltage is above or equal to the reference voltage as opposed to just being equal to it. Both asynchronous sensing and nonlinear control are integrated in a basic digital LDO topology to retain a wide operational current and voltage range.

In section II, we explain the motivation and operation of asynchronous non-linear control. In section III, the architecture and design of the digital LDO are presented followed by measurement results from a test-chip built in 65nm CMOS process and conclusion.

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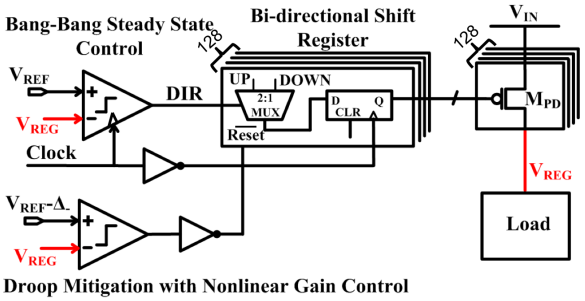

Fig. 1. Architecture of the proposed digital LDO.

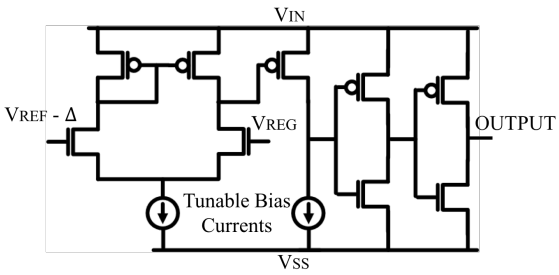

Fig. 2. Design of asynchronous continuous-time comparator.

II. Motivation and Operation of Asynchronous Non-linear Control

A. Asynchronous Voltage Droop Detection

The operation of a basic digital LDO utilizes a master clock to sense and actuate power transistors as shown in Fig. 1. It has been well established that increasing clock frequency at iso-load condition makes the LDO loop underdamped. It results in long settling time after a load transient due to decreased phase margin and a large voltage ripple in steady-state. Ultimately unstable behavior or loss of regulation can occur if the clock frequency is increased to a very high value. Therfore, an upper limit on the operational clock frequency limits the maximum achievable transient performance which is of tantamount importance in digital circuits with small decoupling capacitor budget.

As a solution, voltage droop detection using a clock-less comparator in high performance modes decouples the transient performance of the LDO from the master clock frequency. Biased clock-less comparators can outperform sense amplifier based comparators at high voltages where load transients also exhibit large changes [6]. As the supply voltage goes down, the magnitude of load current steps also decreases and regular droop detection techniques can be employed.

B. Non-linear Control

In the proposed non-linear control, all the power transistors of the digital LDO are asynchronously turned on when a voltage droop is detected. This results in maximum voltage droop mitigation as compared to any other control action which turns on a lesser number of power transistors. Due to this non-linear droop mitigation, a large mismatch between load and supply current can induce an unfavorable large overshoot. The clamping effect of the power transistors and enough decoupling capacitor on the supply node will keep the overshoot equal or below the supply voltage.

Nevertheless, this nonlinear action results in extra power losses approximated as

$$P_{LOSS} = C_{g'} V_{DD}^2 / T_s + C_{LOAD}(V_{DD} - V_{REF})^2 / T_1 \quad (1)$$

$C_{g'}$ is the gate capacitance of surplus power transistors than required by the load and T_s refers to the gate driver rise-time. C_{LOAD} is the load capacitance on the regulated voltage. T_1 is the time difference when regulated voltage reaches its peak value and when it is equal to the reference voltage. Assuming a capacitive load, T_1 is inversely proportional to the load current. Similarly, effective $C_{g'}$ increases as load current decreases. Therefore, the power overhead incurred in the digital LDO operation increases if a small load step triggers the non-linear control action. To prevent unnecessary dynamic power loss, the voltage droop detection threshold must be placed to account for only large load current transients. To guarantee a stable voltage settling after a non-linear control action and the subsequent voltage overshoot, a low frequency master clock must be employed to allow the regulated voltage to return smoothly to reference voltage without any oscillations.

III. Architecture and Design

The basic digital LDO structure is based on the design presented in [2] as shown in Fig. 1. This design offers a simple shift register based control logic which is readily synthesizable as a digital circuit. A sense amplifier based comparator detects the difference between V_{REG} and V_{REF}. If $V_{REG} > V_{REF}$, a single power transistor is turned off by using right shift of all the values in the shift register and if $V_{REG} < V_{REF}$, left shift of all the values is performed. In the current implementation, the power stage comprises of 128 equally sized power MOSFETs controlled through 128-bit shift register. The sense amplifier operates on the positive clock edge followed by shift register action on the following clock edge. This dual edge logic reduces the latency between sampling and actuation of the power stage.

Voltage droop detection is performed using a continuous-time comparator comprising of a two-stage amplifier followed by fast slew rate inverters as shown in Fig. 2. The first stage of the amplifier is an active- loaded differential amplifier. Common-source amplifier based second stage is used to enhance the gain of the comparator. The two-stage amplifier is followed by fast slew rate inverters to increase the driving capability and decrease the latency of the comparator action. Tail current of both the stages of the two-stage amplifier is externally tunable to allow offset and mismatch compensation. The comparator compares V_{REF}-Δ with V_{REG} to determine the voltage droop. In case of a voltage droop, the output of the comparator is propagated as a reset signal to all of the 128 bits of the shift register flip-flops. This action enables all

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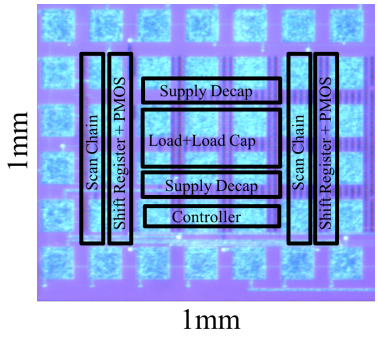

Fig. 3. Chip micrograph with circuit placement details. The testing is performed on a QFN packaged die.

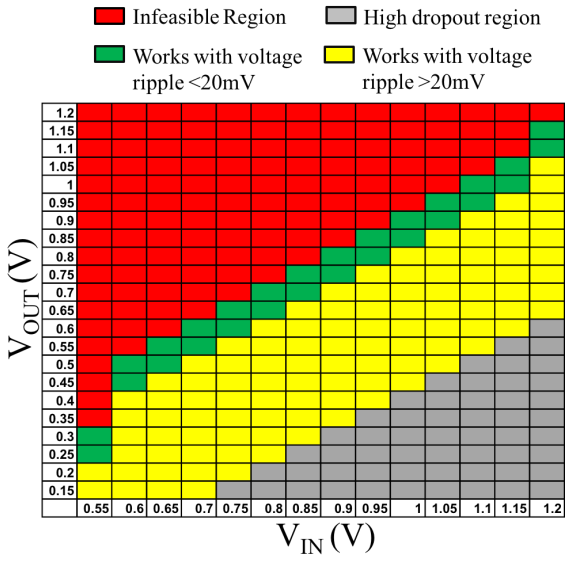

Fig. 4. Shmoo plot showing the wide operational range of the proposed digital LDO. Load current is not constant at different V_{IN} and V_{OUT}.

the power transistors resulting in maximum possible voltage droop mitigation. The comparator topology is kept simple to allow fast decision at minimum possible quiescent current and design overhead.

IV. Measurement Results

The design is fabricated in 65nm CMOS process. The chip micrograph is shown in Fig. 3. The nominal supply voltage for high performance mode is 1.2 V. The LDO is designed to deliver a maximum load current of 125mA at a dropout voltage of 600mV occupying a total area of only 0.061mm^2 excluding decoupling capacitor area.

Fig. 4 presents the shmoo plot showing the operational range of the designed LDO. Given a simplistic low overhead design of the digital LDO, it can operate with a supply voltage from 0.55V to 1.2V. The regulated output voltage ranges from 0.15V all the way up to 1.15V with a minimum operational dropout voltage of only 50mV. To the best of authors′ knowledge, 0.15V is the lowest regulated voltage reported in the literature.

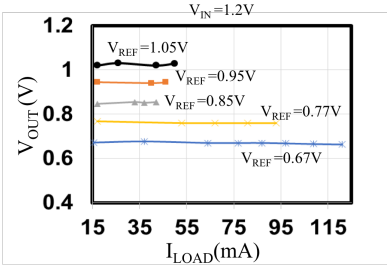

Fig. 5. Measured Load Regulation.

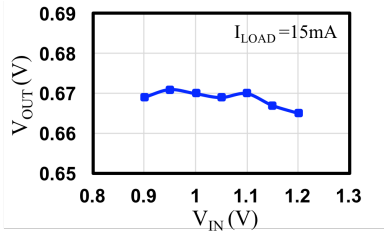

Fig. 6. Measured Line Regulation with V_{REF}=670mV.

For a dropout voltage of greater than 100mV, the steady-state voltage ripple of the design cannot be guaranteed to be less than 20mV. This is because at an increased dropout voltage, the current contribution of each power transistor grows nonlinearly resulting in a larger ripple especially under light load current conditions. Advanced steady-state ripple mitigation techniques like clock adaptation [2] and multiple size power stage quantization [7]–[10] can be readily added to this design but are not discussed given the focus of this publication is on the transient performance.

Load regulation measurements for different dropout voltages are covered in Fig. 5. The straight-line behavior of the curves across different dropout voltages show that load regulation remains constant across a large current range of 15mA to 121mA. Fig. 6 shows line regulation measurements for reference voltage of 670 mV and load current of 15mA when supply voltage varies from 0.9 to 1.2 V. A worst case error of 5mV is measured at the highest dropout voltage.

A comparison of asynchronous non-linear control digital LDO transient performance against a baseline digital only LDO captured on oscilloscope is shown in Fig. 7. The voltage droop reduces by 425mV as compared to the baseline design for a load step of 16 to 53mA in 1μs transition time with C_{LOAD}=1nF, C_{IN}=2nF, V_{REF}-Δ=750mV. The clock is maintained at a low frequency of only 500 KHz showing optimal settling after non-linear recovery from a voltage droop. To account for varying decoupling capacitor budget and load transition rates, as expected in a digital load circuit, the supply capacitance is increased to 1μF and load step transition edge is reduced to only 2ns. Under such a scenario, a voltage droop of approximately 350mV is measured for load step of 44mA as shown in Fig. 8. Package and board resonances due to parasitic inductance contributes to the oscillatory behavior before the

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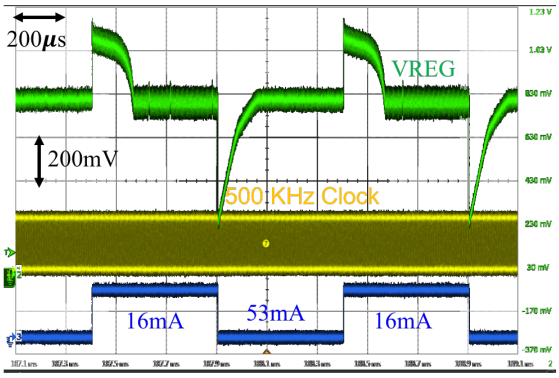
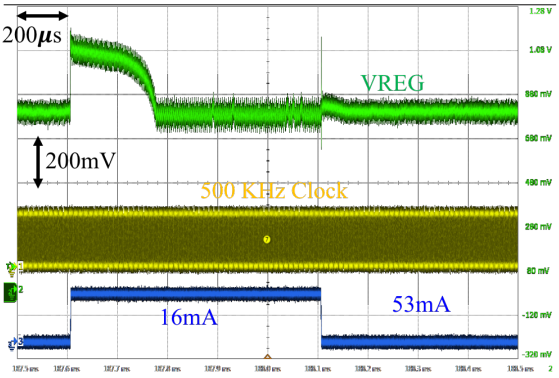


(a)



(b)

Fig. 7. Transient plot showing load step and release for (a) baseline digital LDO (b) proposed digital LDO. V_{REF}=875mV, V_{REF}-Δ=750mV.

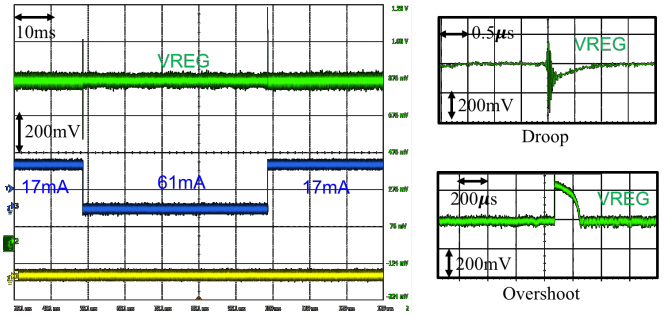


Fig. 8. Transient performance against large load current step and release with asynchronous non-linear control. V_{REF}=875mV, V_{REF}-Δ=750mV.

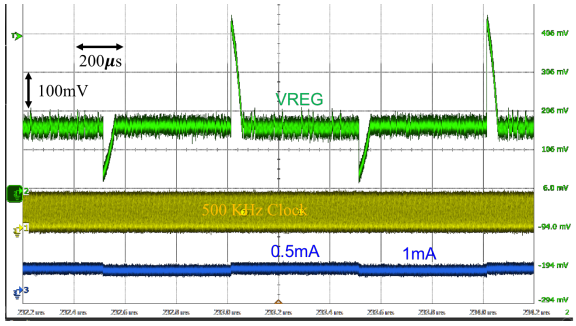


Fig. 9. Transient performance of baseline digital LDO at V_{REF}=150mV and V_{IN}=1.2V.

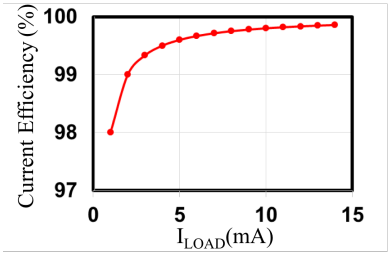


Fig. 10. Measured static current efficiency of the proposed design.

TABLE I
COMPARISON TABLE

	This work	[7]	[8]	[9]	[10]
Type	DLDO with async. non-linear droop mitigation	Async. DLDO	DLDO	DLDO	DLDO
Process (nm)	65	65	40	28	65
V_{IN} (V)	0.55-1.2	0.6-1	0.6-1.1	1.1	0.6-1.1
V_{REG} (V)	0.15-1.15	0.55-0.95	0.5-1	0.9	0.4-1
$I_{LOAD,MAX}$ (mA)	125	500	210	200	100
F_{CLOCK} (MHz)	0.5	-	N/A	N/A	500
C_{LOAD} (nF)	1	1.5	20	23.5	1
C_{IN} (nF)	1-1000	N/A	N/A	N/A	N/A
I_Q (uA)	0-20	300	22.6-98.5	110	82
Load Reg. (V/A)	<0.18	0.25	0.075	N/A	0.06
Area (mm^2)	0.061	0.158	0.192	0.021	0.01
Max Curr. Efficiency (%)	99.99	99.99	99.99	99.94	99.92

voltage settles. These second order effects are not observed for digital LDOs targeting a small current range of a few mA. On the other hand, it proves the importance of designing a robust power delivery network to support high current and fast transient digital LDOs. Low regulation voltage operation of the proposed LDO is measured at 150mV under a load step of 0.5mA, as shown in Fig. 9. At low voltage operation, the droop comparator is non-operational and only the digital LDO is used. A measured quiescent current of only 20μA, mostly consumed by the droop detection comparator, allows a measured current efficiency of greater than 99.5% for just 4mA of load current as shown in Fig. 10. A comparison with current state-of-the-art designs show competitive performance of the proposed LDO as summarized in Table I.

V. CONCLUSION

A wide dynamic range digital low dropout voltage regulator is presented in this paper capable of enabling per-core DVFS. The design uses asynchronous nonlinear control to achieve fast voltage droop mitigation under large load current steps. Measurements on a test-chip built in 65nm CMOS show a load current range of up to 125mA and regulated voltage range of 0.15V to 1.15V from a supply voltage of 1.2V. The design shows greater than 99.5% current efficiency at a light load of only 4mA with 1nF decoupling capacitance.

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