An Empirically Validated Virtual Source FET Model for Deeply Scaled Cool CMOS

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***Abstract*—**In this work we extend the compact Virtual Source (VS) model for nanoscale MOSFET from room temperature to 6K to advance the development of an ultra-compact model for low temperature CMOS (Cool-CMOS) technology. To achieve this we characterize 30 nm channel length bulk-Si CMOS FETs from 300K to 6K and extract the VS model parameters to investigate the ballistic efficiency of nanoscale FETs as a function of temperature. We conclude that while ballistic efficiency of nanoscale MOSFETs degrade in linear region as we approach cryogenic temperature, its ballistic efficiency improves in the saturation region at low temperature. Parametric V_{DD} sweeps show that the VS model is also ready for use in low power cryogenic circuit design. Finally, the model is used to project performance of Cool CMOS technology for 15nm channel length FETs at deeply scaled nodes and prove its viability for use.

I. Introduction

MOSFETs operating at cryogenic temperature (Cool-CMOS) finds variety of applications from high performance computing in data centers, to sensor interface circuits in space-crafts to Q-bit controller circuits in quantum processors (Fig 1). Trust-worthy physics-based compact models for deeply scaled MOSFETs operating at cryogenic temperature are necessary to bridge the gap between the devices and systems operating at cryogenic temperature. Hence it is extremely important to understand the temperature dependent physics of electrostatics and transport in nanoscale MOSFETs. In this work we develop an intuitive and quantitative understanding of the ballistic and quasi-ballistic nature of the transport phenomena in extremely scaled MOSFETs as a function of temperature and their critical dependence on electrical bias conditions. We use the modified VS model to study the effects of supply voltage and channel length scaling on the ballisticity for Cool CMOS.

II. Cool CMOS Virtual Source Model

The VS model is a semi-empirical physics based compact model which covers diffusive, quasi-ballistic and ballistic transport in nanoscale MOSFETs. The virtual source is assumed to be located at the top of the gate-controlled energy-barrier from where the carriers get thermally injected into the channel with an injection velocity (v_{inj}). Hence, the drain current (I_D) in the channel can be computed as the product of the mobile charge density (Q_{inv}) and injection velocity at the VS point as:

$$I_D = W Q_{inv} v_{inj} F_{sat} \quad (1)$$

where W is the geometric device width and F_{sat} is an empirical function that smoothens the transition from linear to saturation regimes. For a transistor operating at its ballistic limit carrier injection velocity is equal to the thermal velocity (v_T). Typically, even in nanoscale MOSFETs, only a fraction of total injected carriers propagate towards the drain, whereas the rest of the carriers back-scatter in the channel and are sent back to the source. This back-scattering theory allows to express the carrier transport mechanism in the channel for both linear and saturation region of operation as listed in Table I [1]. The ballistic efficiency of a nanoscale MOSFET can also be estimated as mentioned in Eq. (4) and Eq. (7) in Table I. The VS model requires only a set of 12 input parameters to fit the experimental data amongst which 6 physical parameters can be directly obtained from the experiments. To investigate and incorporate the underlying temperature-dependent physics of nanoscale MOSFETs in the VS model for Cool CMOS, we characterize both short channel NMOS and PMOS from 300K to 6K to extract the required physical parameters.

III. Experimental Characterization Of Cool CMOS

Bulk Si-CMOS devices with channel length (L_G) of 30 nm were characterized. The saturation ($|V_{DS}|$=0.8V) and linear ($|V_{DS}|$=50mV) transfer characteristics, and the output characteristics were measured from 300K to 6K. The threshold voltages ($V_{th,Lin}$) for both NMOS and PMOS increase monotonically with decreasing temperature (Fig 2a), However, DIBL in NMOS is relatively more sensitive to temperature (Fig 2b). The sub-threshold swing (SS) improves monotonically from 300K till 6K for both NMOS and PMOS as shown in Fig 2c. However it should be noted that SS only decreases to 20mV/dec for both NMOS and PMOS at 6K, whereas the theoretical limit is 1.2mV/dec. Thus, the n-factor ($SS/SS_{Theoretical}$), sharply increases at low temperature due to band-edge interface traps and change in the Fermi-occupation function at low temperature [2]. The series resistance is extracted at all temperatures using the y-function method [3]. The series resistance improves by 1.2x for both PMOS and NMOS at 6K compared to 300K. The above temperature dependent device parameters are used to fit the transfer characteristics and output characteristics at each temperature (Figs 3a-d). Excellent agreement between measured data and the VS model is obtained. This enables accurate extraction of various transport parameters (μ_{app} and v_{inj}) for all the temperatures and this temperature dependence are studied extensively in the following section.

IV. Temperature Dependent Transport Parameters In Cool CMOS

Low Tempeature Transport in Linear Region

Under low drain bias, the mobility extracted from the VS model is referred to as the apparent mobility (μ_{app}) [1], which is a combination of effective mobility in the diffusive limit and the ballistic mobility at a given temperature as given by Eq. (10) in Table I. As the temperature decreases, the extracted value of μ_{app} initially increases for both NMOS and PMOS up-to a temperature T_m (150K in this case) and then decreases as the temperature is further lowered (Fig 4.a). The contribution of effective mobility (μ_{eff}) is evaluated using Eq. (10) in Table I, which also shows a similar trend as μ_{app} (Figs 4b-c). It is to be noted that the power law dependence of both μ_{app} and μ_{eff} are almost similar for PMOS and NMOS which suggests similar scattering mechanisms dominating transport in both at a given temperature. Temperature dependence of μ_{eff} ($\sim T^{-1.45}$) below T_m suggests that the transport is limited by phonon scattering which reduces with decreasing temperature. But as the temperature is decreased further, a strong degradation in μ_{app} is observed which is interpreted as an increasing contribution from ionized impurity scattering from the high doping density in the channel provided by halo implantation in bulk Si CMOS. This is further validated by extracting the average mean-free path for back-scattering (λ) as expressed in Eq. (11) in Table I. It is observed that though λ increases initially with decreasing temperature due to reduced phonon scattering, it eventually degrades at low temperature (Fig 5.a). The temperature dependence of λ is also reflected in the linear ballistic ratio (Γ_{Lin}) as shown in (Fig 5b), defined as [λ/ (λ+L)] where L is the effective channel length. Hence the extraction of μ_{app} from VS model suggest that though short-channel bulk devices operate at a higher ballisticity compared to room temperature for $T > T_m$, the device moves away from its ballistic limit at low temperature under low drain bias due to increased back-scattering from impurity scattering in the channel.

Low Tempeature Transport in Saturation Region

Carrier transport in saturation region follows a slightly different mechanism than linear region [1]. As shown in Figs 6a, b, the extracted injection velocity (v_{inj}) decreases with temperature which is in perfect agreement with the fact that the thermal injection velocity also decreases with temperature (Eq. 8 in Table I). The extracted v_{inj} shows weaker temperature dependence ($\sim T^{0.18}$ for NMOS and $\sim T^{0.15}$ for PMOS) in comparison to the ballistic thermal injection velocity ($\sim T^{0.5}$) which indicates that, despite increased back-scattering in the low field region under high applied V_{DS}, the device moves closer to its ballistic limit at low temperature. While diffusing through the low-field region of the channel, the fraction of injected carriers that energy more than kT are not likely to returning to the source even in the event of back scattering and eventually get absorbed into the drain. Hence, the backscattering occurs within a distance of kT energy-drop from the top of the barrier (L_{kT}) as depicted in Fig 7a. Now with decreasing temperature the L_{kT} length also decreases linearly (Fig 7.b). Hence, at low temperature, the L_{kT} length is almost negligible in comparison to λ and less fraction of the injected carriers are scattered back into the source. The saturation ballistic ratio (v_{inj}/v_T) hence increases at low temperature and approaches unity at 6K (Fig 7.b). Thus, the extraction of v_{inj} from compact virtual source model suggests that nanoscale MOSFETs operate close to its ballistic limit at cryogenic temperature in the saturation region.

V. Effects of Supply Voltage and Channel Length Scaling on Ballisticity

Here, we investigate the effect of supply voltage (V_{DD}) and channel length (L_G) scaling on ballistic efficiency of Cool CMOS using the VS model at different temperature.

A.Effects of Supply Voltage on the ballisticity

As shown in Figs 8a, b, injection velocity is more sensitive to change in V_{DD} at 300K but becomes a weak function of V_{DD} at 6K. Consequently we see the same trend in saturation ballistic ratio as the ballisticity in the device saturates at lower temperature with V_{DD} (Fig 9.a). Lower sensitivity of v_{inj} to V_{DD} is caused by the negligible change in L_{kT} length with change in V_{DD} (Fig 9.b) at low temperature where V_{DD}>>kT/q. This also allows to scale the supply voltage more at low temperature compared to room temperature for matched I_{OFF} and same performance.

B. Effects of Channel Length on the ballisticity

Finally, we use the modified VS model to predict the transfer characteristics of MOSFETs with shorter channel lengths, considering short channel effects at a fixed I_{OFF} (Fig. 10). The 15 nm channel length device shows a higher SS compared to other channel lengths at room temperature as expected due to worse short channel effects. But, at lower temperature the improvement in SS allows the 15nm channel length device to recover most of the performance loss. The channel length scaling reduces the μ_{app} as μ_B reduces for shorter channel lengths (Table I, Eq. (9)), however, no degradation in μ_{app} is observed at 6K (Fig 11), as it is dominated by channel length independent μ_{eff} at low temperature. Figs 12a-b show that both v_{inj} and ballistic ratio show no further improvement at low temperature, hence the benefit in saturation current in 15nm devices solely comes from the improvement in SS.

VI. Conclusion

In this work we incorporate the temperature dependency of electrostatic and transport parameters as well as external resistance within the compact physics based Virtual Source model parameters to investigate and reproduce the response of nanoscale MOSFETs fabricated on bulk-Si down to 6K as listed in Table II. We perform extensive characterization on 30 nm bulk-Si CMOS down to 6K and extract the VS Model parameters that enable us to capture the ballistic efficiencies of low and high drain bias transport at cryogenic temperature. We provide an intuitive yet quantitative understanding of the difference in transport mechanisms under different drain bias and explore the effect of channel length and supply voltage scaling to enable low voltage cryogenic circuit design and performance projection of Cool CMOS for 15nm channel length FETs at deeply scaled nodes.

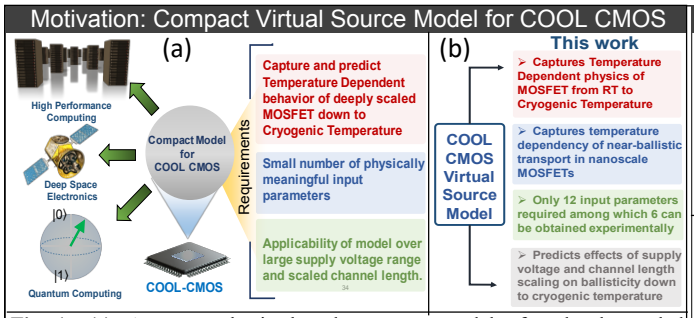
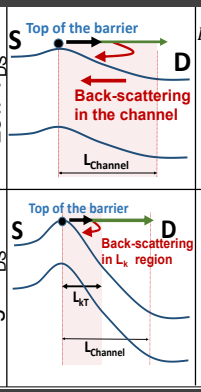


Fig 1: (a) Accurate physics-based compact models for deeply scaled MOSFETs operating at cryogenic temperature needed (b) Cool-CMOS Virtual Source model id developed to capture the temperature dependency of ballistic and quasi-ballistic transport in nanoscale MOSFETs.

Table I : Equations of Virtual Source Model



$$I_{DLIN} = \frac{W}{L}\mu_{app}|Q_n(V_{GS},V_{DS})|V_{DS} \quad (2)$$

$$\mu_{app} = \frac{\Gamma_{Lin}Lv_T}{2kT/q} \quad (3)$$

$$\Gamma_{Lin} = \frac{\lambda}{\lambda + L} \quad (4)$$

(Linear Ballistic Ratio)

$$I_{DSAT} = W|Q_n(V_{GS},V_{DS})|v_{inj} \quad (5)$$

$$v_{inj} = \Gamma_{Sat}v_T \quad (6)$$

$$\Gamma_{Sat} = \frac{\lambda}{\lambda + 2L_{kT}} \quad (7)$$

(Saturation Ballistic Ratio)

$$v_T = \frac{2kT}{\pi m^*}\frac{F_{1/2}}{F_0} \quad (8)$$

$$\mu_{Ballistic} = \frac{v_T L}{2kT/q} \quad (9)$$

$$\frac{1}{\mu_{app}} = \frac{1}{\mu_{eff}} + \frac{1}{\mu_{Ballistic}} \quad (10)$$

λ: *MFP for back-scattering*

$$\lambda = \frac{2kT\mu_{eff}}{qv_T}\frac{F_0}{F_{-1/2}} \quad (11)$$

Experimental Characterization of Cool CMOS

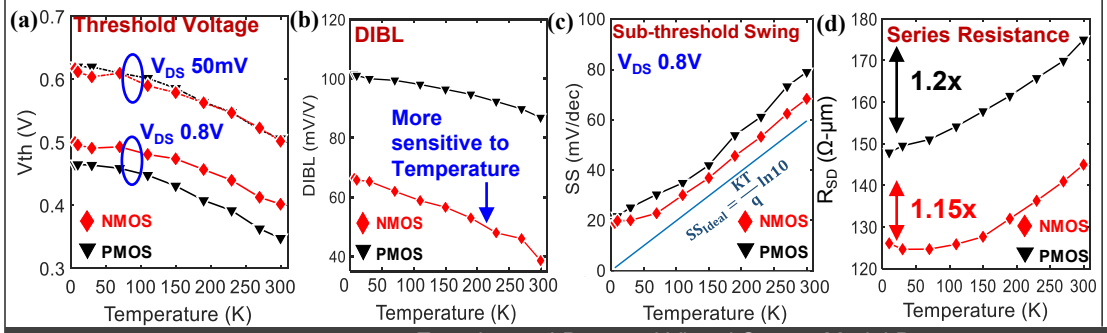


Fig 2: (a) V_{th} increases at lower T for both NMOS and PMOS; (b) DIBL increases more at lower temperature for NMOS; (c) SS decreases at low T but deviates more from its theoretical value at cryogenic temperature due to occupation of band-edge interface traps; (d)Series resistance extracted by Y-function method shows 1.2x and 1.15x improvement at low temperature for PMOS and NMOS respectively.

Experimental Data and Virtual Source Model Data

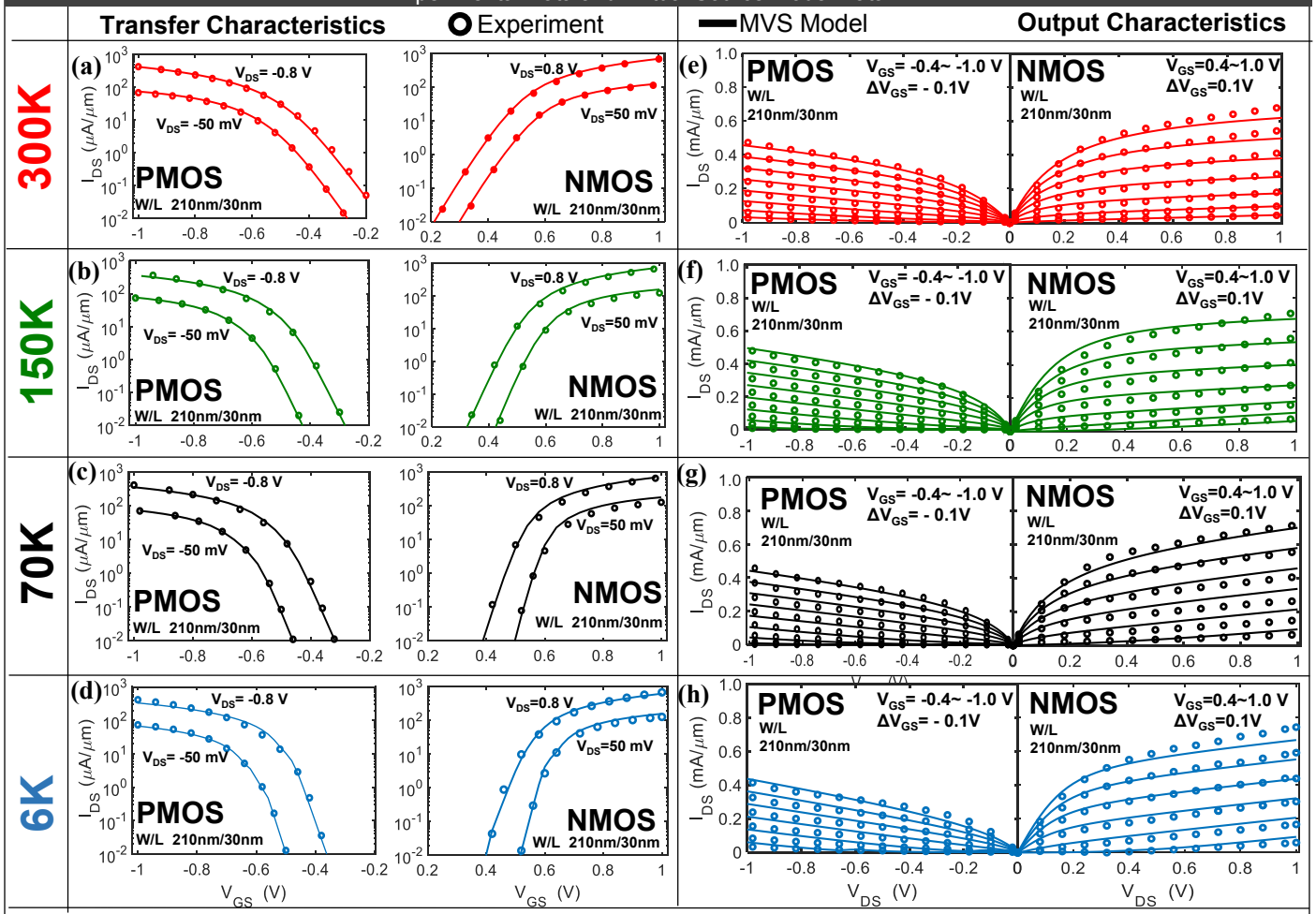


Fig 3: Experimental data from 30 nm bulk-Si CMOS device along with VS model data; Transfer Characteristics at (a) 300K, (b) 150K, (c) 70K, (d) 6K for $|V_{DS}|$=0.05V and 0.8V; Output Characteristics at (e) 300K, (f) 150K, (g) 70K, (h) 6K

Parameter Extraction using MVS Model in Linear Region (V_{DS}= 50 mV)

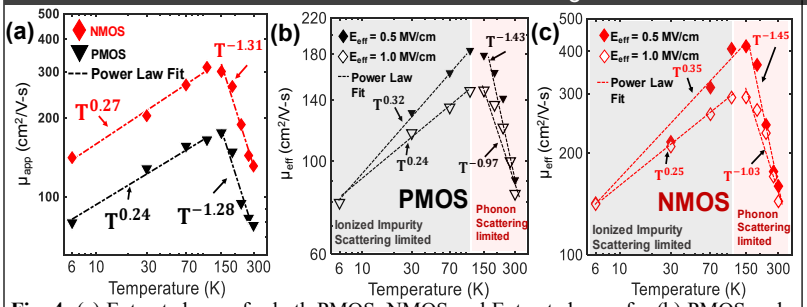


Fig 4: (a) Extracted μ_{app} for both PMOS, NMOS and Extracted μ_{eff} for (b) PMOS and (c) NMOS initially increases with decreasing temperature due to reduced phonon scattering but further decreases due to ionized impurity scattering from high channel doping density by halo implantation.

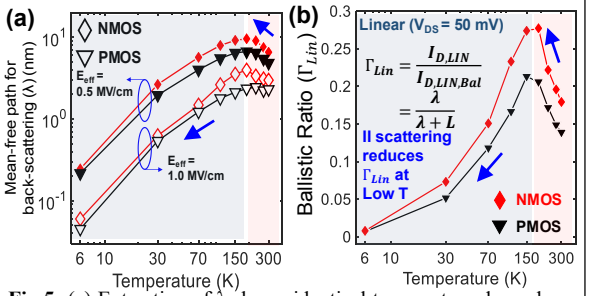


Fig 5: (a) Extraction of λ shows identical temperature dependence as observed for μ_{eff} (b) Device moves away from its ballistic limit at low temperature under low drain bias as back-scattering of carriers increase in the channel

Parameter Extraction using MVS Model in Saturation Region (V_{DS}= 0.8 V)

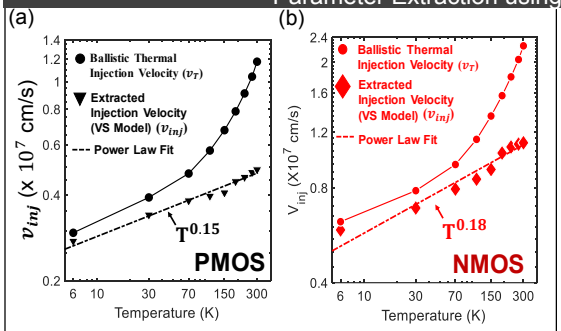


Fig 6: v_{inj} decreases with a weaker temperature dependence compared to v_T (~$T^{0.5}$) in (a) PMOS v_T (~$T^{0.15}$) and (b) NMOS v_T (~$T^{0.18}$) and approaches v_T at very low temperature below 30K.

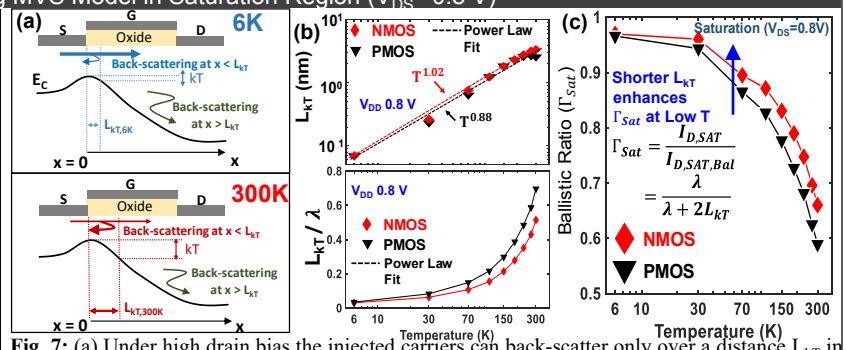


Fig. 7: (a) Under high drain bias the injected carriers can back-scatter only over a distance L_{kT} in the channel (b) L_{kT} shows linear dependence with temperature and becomes negligible compared to λ (L_{kT}/ λ << 1) at low temperature. Consequently (c) nanoscale MOSFETs operate close to its ballistic limit in saturation region at 6K

Effect of Supply Voltage Scaling at Low Temperature

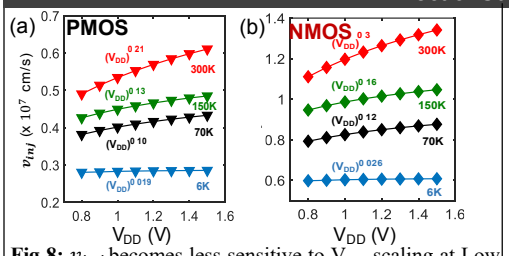


Fig 8: v_{inj} becomes less sensitive to V_{DD} scaling at Low temperature in comparison to 300K for both (a) PMOS and (b) NMOS

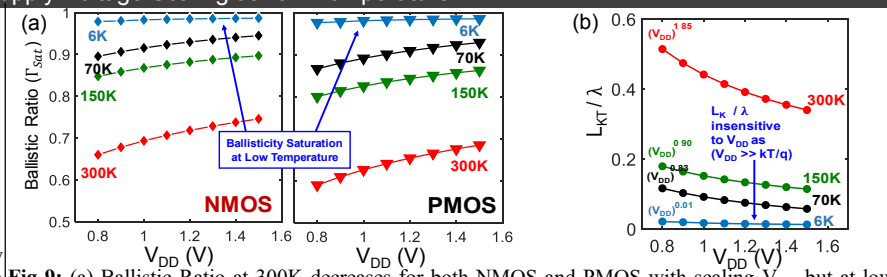
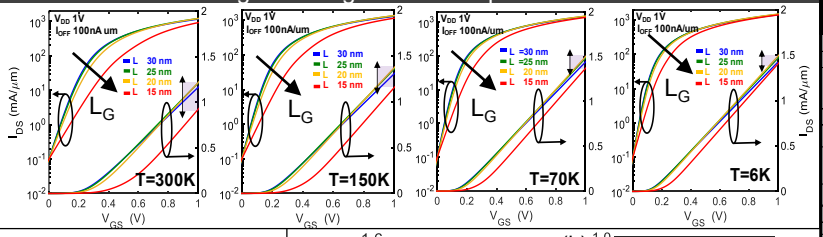


Fig 9: (a) Ballistic Ratio at 300K decreases for both NMOS and PMOS with scaling V_{DD} but at low temperature it remains close to unity due to (b) negligible change in L_{kT} / λ with V_{DD} at low temperature

Effects of Channel Length Scaling at Low Temperature

Fig 10: Transfer characteristics of MOSFETs with different channel length simulated using Cool-CMOS VS Model



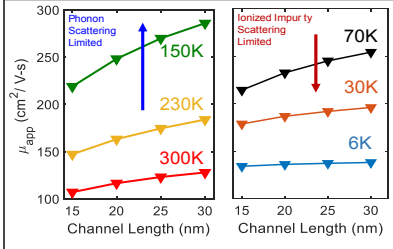


Fig 11: μ_{app} reduces for shorter channel lengths but remains almost constant for 6K, limited by channel length independent effective mobility.

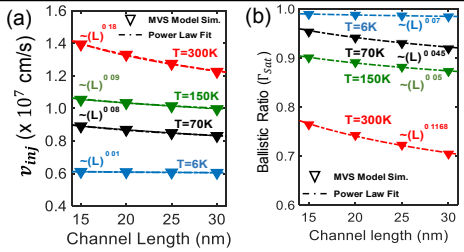


Fig 12: At room temperature **(a)** v_{inj} **(b)** Γ_{Sat} improve with scaling channel length but remain unchanged at low temperature

Table II

Temperature Dependence of Device Parameters in Bulk COOL-CMOS VS Model

		NMOS	PMOS
Extrinsic Parameter			
Series Resistance (RSD)		$T^{1.6}$	$T^{2.6}$
Intrinsic Parameter: Electrostatics			
n-factor (n_0)		$T^{-1.07}$	$T^{-0.93}$
Threshold Voltage ($V_{th,Lin}$)		$T^{-1.62}$	$T^{-1.7}$
DIBL		$T^{-1.8}$	$T^{-1.3}$
Intrinsic Parameter: Transport			
T_M=150K (in this work)		$T>T_M$ / $T<T_M$	$T>T_M$ / $T<T_M$
Apparent Mobility (μ_{app})		$T^{-1.3}$ / $T^{0.27}$	$T^{-1.28}$ / $T^{0.24}$
Effective Mobility (μ_{eff})	Low Field (0.5MV/cm)	$T^{-1.43}$ / $T^{0.32}$	$T^{-1.45}$ / $T^{0.35}$
	High Field (1MV/cm)	$T^{-0.97}$ / $T^{0.24}$	$T^{-1.03}$ / $T^{0.35}$
Injection Velocity (v_{inj})		$T^{0.15}$	$T^{0.18}$

Comparison between different COOL-CMOS Models

	Drift Diffusion based COOL CMOS Model [4]	EKV based COOL CMOS Model[5]	This Work
Compact Model	NO	YES	YES
Applicability to NanoMOSFE s	NO	YES	YES
No of Input parameters	–	< 20	< 10

References: ***[1]****M.Lundstrom et al, TED 2014;* ***[2]****W.Chakraborty et al,DRC 2019;* ***[3]*** *R. Trevisoli et al, TED 2017;* ***[4]****A.Beckers et al,TED 2018;* ***[5]****A.Beckers et al,EDS 2016*