

# NeuroSLAM: A 65-nm 7.25-to-8.79-TOPS/W Mixed-Signal Oscillator-Based SLAM Accelerator for Edge Robotics

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**Abstract**—Simultaneous localization and mapping (SLAM) is a quintessential problem in autonomous navigation, augmented reality, and virtual reality. In particular, low-power SLAM has gained increasing importance for its applications in power-limited edge devices such as unmanned aerial vehicles (UAVs) and small-sized cars that constitute devices with edge intelligence. This article presents a 7.25-to-8.79-TOPS/W mixed-signal oscillator-based SLAM accelerator for applications in edge robotics. This study proposes a neuromorphic SLAM IC, called NeuroSLAM, employing oscillator-based pose-cells and a digital head direction cell to mimic place cells and head direction cells that have been discovered in a rodent brain. The oscillatory network emulates a spiking neural network and its continuous attractor property achieves spatial cognition with a sparse energy distribution, similar to the brains of rodents. Furthermore, a lightweight vision system with a max-pooling is implemented to support low-power visual odometry and re-localization. The test chip fabricated in a 65-nm CMOS exhibits a peak energy efficiency of 8.79 TOPS/W with a power consumption of 23.82 mW.

**Index Terms**—Accelerator, continuous attractor network, edge intelligence, experience map, simultaneous localization and mapping (SLAM), spiking neural network (SNN), topological map, visual odometry, visual template (VT).

## I. INTRODUCTION

THE ever-increasing demands on widespread applications in autonomous navigation such as in mobile robotics, self-driving vehicles, and unmanned aerial vehicles (UAVs) have piqued our interest in recent years. Due to the advent of autonomous navigation, technologies on estimating self-motion of agents and filtering the cumulative error while observing an environment have become essential [1], [2]. The problem of self-motion estimation and error filtering has been studied in robotics as simultaneous localization and mapping (SLAM). SLAM is a quintessential problem in autonomous navigation with applications in obstacle avoidance, path planning, and swarm robotics [3]–[8]. Visual SLAM using a

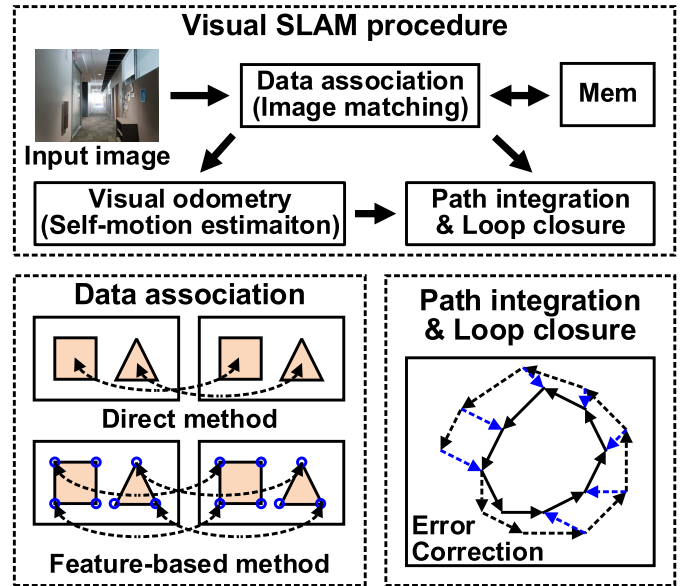


Fig. 1. Simplified procedure of the visual SLAM operations.

monocular or stereo camera has been widespread [9], [10] because of its low cost and simple platform integration. In visual SLAM, an inertial measurement unit or an RGB-D camera can be also employed tradingoff between accuracy and power consumption [11]–[14]. Recently, low-power visual SLAM operation has gained importance with applications in power-limited edge devices such as UAVs and small-sized cars with edge intelligence. Since the SLAM on the battery-powered edge devices has a strict power budget, the dedicated visual SLAM system is necessary for application in edge robotics. Fig. 1 depicts a simplified procedure of the visual SLAM operation. In visual SLAM, the self-motion of an agent and re-localization are conducted with input images. Data association determines whether an input image is matched with previously observed images stored in a memory. For image matching, a direct or a feature-based method can be employed. A direct method conducts the data association based on the difference of pixel data which is called a photometric error. A feature-based method extracts distinct points, called features, and compares features in each image. In case an input image is not matched with the retained images, the visual SLAM stores the input image as well the information of the current position of the agent in the memory for future data association. Visual odometry estimates the self-motion

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of the agent considering the change of images from one frame to the next. Then, path integration is performed by accumulating the output of the visual odometry system. Since the output of the visual odometry inevitably contains an error in estimating the self-motion, the error is accumulated during path integration. In order to suppress the accumulated errors, loop closure is employed in visual SLAM. In case an input image is matched with any of the retained images in the phase of data association, the agent recalls the corresponding position considering the matched image from the memory and loop closure occurs to correct the error accumulated during path integration.

As a solution to the visual SLAM, computational methods have long been studied [15], [16]. Probabilistic SLAM such as Kalman filter-based SLAM represents the position of an agent and distinct objects in the environment, called landmarks, as probabilities. Since probabilistic SLAM requires extensive computation to estimate the probabilities that each object exists in a certain position in every input frame, it is not practical to implement the probabilistic SLAM system on a low power application-specified integrated circuits (ASICs). In pursuit of practical SLAM systems, many prior arts have focused on keyframe-based visual SLAM [17]–[22]. The keyframe-based SLAM estimates the position of the agent in an intermittent frame which is called a keyframe. The keyframe is set to avoid excessive computation while achieving the appropriate SLAM results. Some prior arts that employ keyframe-based SLAM also use feature-based data association. A feature-based method is tolerant of image distortion in estimating the self-motion of the agent. However, since features should be extracted by feature descriptors such as scale-invariant feature transform (SIFT), speeded up robust features (SURF), etc., it leads to computation overhead [23]–[25]. In addition, the distance from the agent across multiple features should be estimated, which incurs a considerable amount of computation. In order to surmount the high power consumption in such SLAM techniques, recent publications employ power-efficient multiply-accumulate (MAC) accelerators [18] for efficient data processing. However, for applications in battery-operated edge robotics, power consumption is severely constrained. Notwithstanding the efforts for designing energy-efficient accelerators, the total power consumption is still high for edge devices. Thus, ultra-low-power edge robotics necessitates not only circuit solutions but also novel algorithms that can significantly reduce the overall system power consumption.

To address the challenge, we explore a different approach from the prior arts. We observe that biological systems can solve SLAM with extreme energy-efficiencies by employing methods that are robust, flexible, and well-integrated into the creatures' sensory systems. Particularly, rodents have shown this extraordinary ability to store and organize visual cues so that a brief sequence of visual cues can globally re-localize the animal. Furthermore, the neural recordings of the rodent hippocampus have led to the discovery of place cells and head direction cells which show striking correlation with mapping tasks [26]. Place cells and head direction cells represent the position and the head direction of a rodent, respectively. Fig. 2 shows the excitation of place cells and head direction

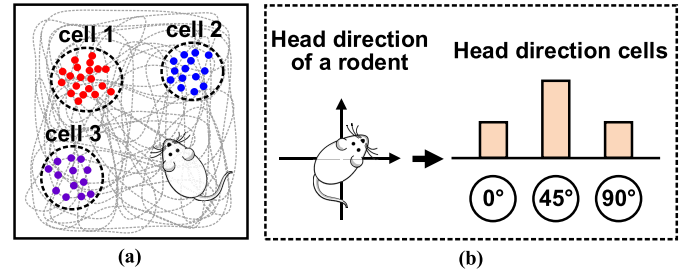


Fig. 2. Excitation of (a) place cells and (b) head direction cells.

cells. In case a rodent is placed at a certain position, a designated place cell is excited. Similarly, head direction cells corresponding to the head direction of the rodent are excited. In place cells and head direction cells, the energy spreads to the adjacent cells through cell-level excitatory coupling, thereby composing a group of excited cells. Furthermore, neurobiological experiments on neural recordings have demonstrated that rodents update and re-localize the position of a group of excitation in place cells and head direction cells considering the self-motion estimation and visual information. In light of the spatial cognition of rodents, RatSLAM was proposed as a bio-inspired SLAM algorithm mimicking place cells and head direction cells of rodents [27], [28]. However, RatSLAM, being an algorithm did not explore the connection between bio-inspired hardware and neuro-inspired algorithms. Instead, RatSLAM has been digitally implemented in CPUs with high power consumption. RatSLAM and recent advances in event-based bio-mimetic hardware inspire us to investigate NeuroSLAM where an oscillatory-neural network can enable an ultra-low-power implementation of SLAM.

In this article, a NeuroSLAM accelerator IC is proposed to support ultra-low-power visual SLAM applications in edge robotics [29]. The NeuroSLAM IC is the first bio-inspired SLAM IC employing the principles of spatial cognition of rodents while considering hardware-efficient designs. The NeuroSLAM IC employs oscillator-based pose-cells and a digital head direction cell to mimic place cells and head direction cells in a rodent brain, respectively. An oscillator array acts as a spiking neural network (SNN) that enables a continuous attractor to mimic the neural activities in pose-cell arrays. In the rest of this article, the oscillator array and SNN are used interchangeably to describe the operation of the pose-cell array. Furthermore, a lightweight vision system with max-pooling is implemented to support low-power visual odometry and re-localization. We demonstrate a test-chip performing visual SLAM with an energy efficiency of 7.25–8.79 TOPS/W where the power consumption is 17.27–23.82 mW, respectively.

The rest of this article is organized as follows. Section II introduces the nature of the spatial cognition of rodents. Section III describes the architecture of the proposed NeuroSLAM accelerator IC. Section IV discusses the detailed implementation of the NeuroSLAM front-end. Section V delineates the mixed-signal oscillator-based pose-cell array in the NeuroSLAM accelerator. Section VI presents the measurement results. Section VII presents the conclusions drawn from this study.

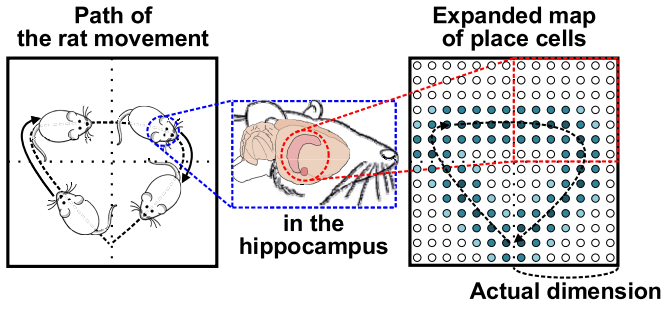


Fig. 3. Mapping between the position of a rodent and the excited place cells in rodent hippocampus.

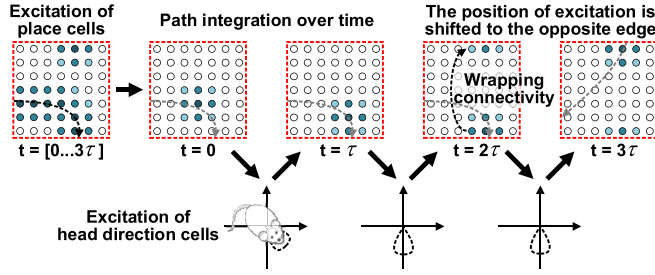


Fig. 4. Path integration with wrapping connectivity in place cells.

## II. SPATIAL COGNITION OF RODENTS

Place cells and head direction cells, which are arranged in a grid, encode spatial location in rodents. Fig. 3 illustrates the mapping between the position of a rodent in an environment and the excited place cells in the rodent hippocampus. Owing to the mapping between place cells and the environment, a rodent can recognize its own position including the path that a rodent explores. The spatial cognition of rodents comprises path integration and re-localization with visual information. Fig. 4 shows the path integration over time in place cells and head direction cells. Considering visual information, path integration occurs by exciting the corresponding place cells and head direction cells. It is noteworthy that the number of place cells is not sufficient to compose a one-to-one mapping to the environment since the dimension of the environment is virtually unlimited. Thus, place cells feature wrapping connectivity to represent the environment within the limited number of place cells. In case an excitation in place cells approaches an edge of place cells during path integration, the excitation is shifted to the opposite edge of the place cell array, thereby continuously tracking the self-motion of the rodent. Owing to wrapping connectivity, a rodent can recognize its position with the finite number of place cells while exploring vast environments. Fig. 5 depicts the cumulative errors in path integration and the re-localization with visual cues. While exploring environments, rodents organize visual cues combined with the location where the visual information is observed. In case a rodent recognizes certain visual information that had been observed before, the re-localization is initiated in the rodent hippocampus. With consecutive observations of the visual cues, a rodent eventually recognizes its correct position via conflict resolution and updates the excitation in the place cells and head direction cells.

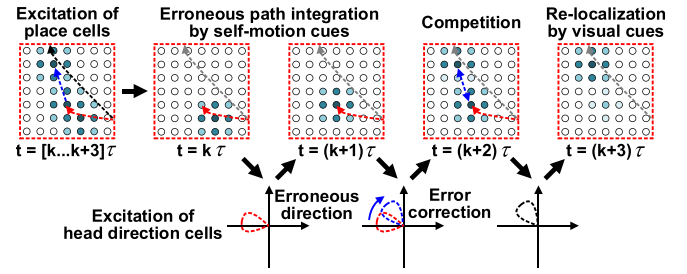


Fig. 5. Erroneous path integration and re-localization with visual cues.

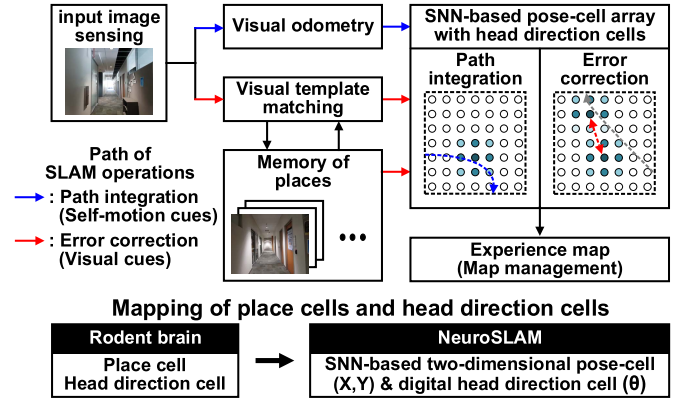


Fig. 6. Architecture of the NeuroSLAM.

## III. PROPOSED NEUROSLAM ACCELERATOR

The NeuroSLAM accelerator employs a similar principle for spatial cognition similar to RatSLAM [28]. Fig. 6 shows the architecture of the NeuroSLAM accelerator. Compared to the RatSLAM which mimicked place cells and head direction cells by employing a 3-D pose-cell array, the NeuroSLAM features a 2-D mixed-signal SNN-based pose-cell array coupled with digital head-direction computation to attain the power-and-area-efficient SLAM system. Since the pose-cell array has wrapping connectivity, a certain pose-cell is excited for multiple positions in the environment. Thus, an experience map is used to represent a unique position of an agent. Fig. 7 shows the architectural block diagram of the proposed NeuroSLAM accelerator. The NeuroSLAM accelerator comprises the image buffer, 1-D-image-based visual odometry, visual template (VT) matching circuits, a VT matching classifier, two banks of on-die SRAM for VT storage, a pose-cell controller including a digital head direction cell ( $\theta$ ), and a  $7 \times 7$  SNN-based circularly connected pose-cell array ( $X, Y$ ) mimicking the attractor properties of the continuous neural network. A pose-cell is connected with adjacent pose-cells, and the edge of the pose-cell array is circularly connected considering the wrapping connectivity. The energy in the pose-cell array is represented by the frequency of the oscillator in each pose-cell. The pose-cell controller is integral to the entire process of the NeuroSLAM accelerator. Fig. 8 shows the simplified system timing diagram of the NeuroSLAM accelerator. The pose-cell controller operates at  $1/16$  of the maximum frequency of the oscillator that is a replica of the oscillator in the pose-cell. Once the input image is ready at the image buffer, the visual



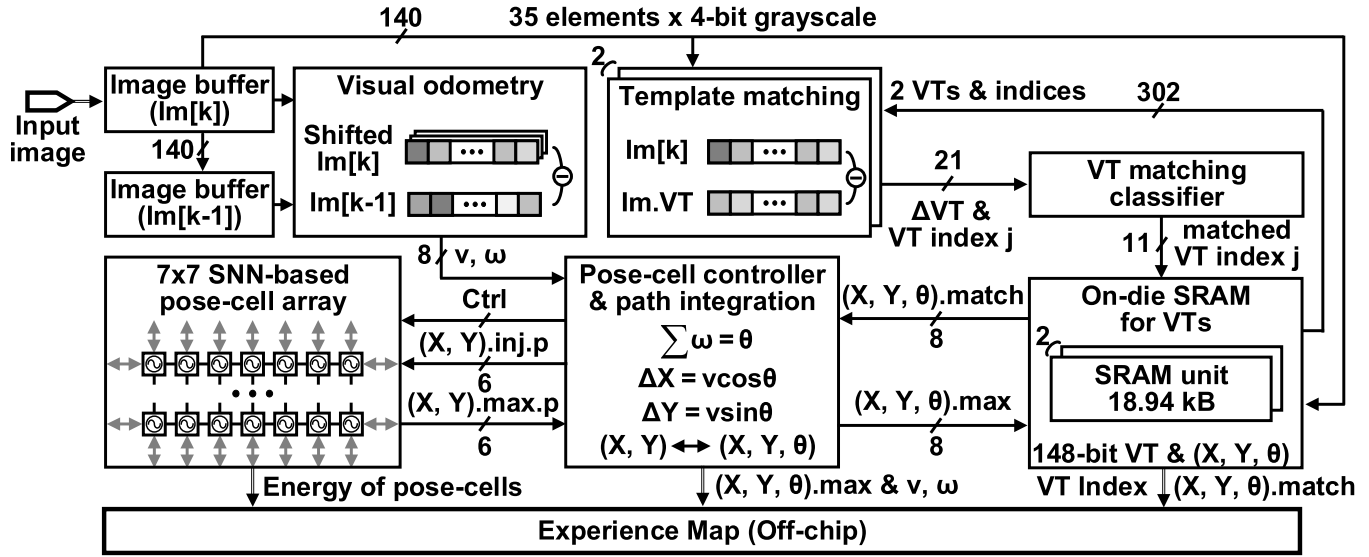


Fig. 7. Top block diagram of the proposed NeuroSLAM accelerator.

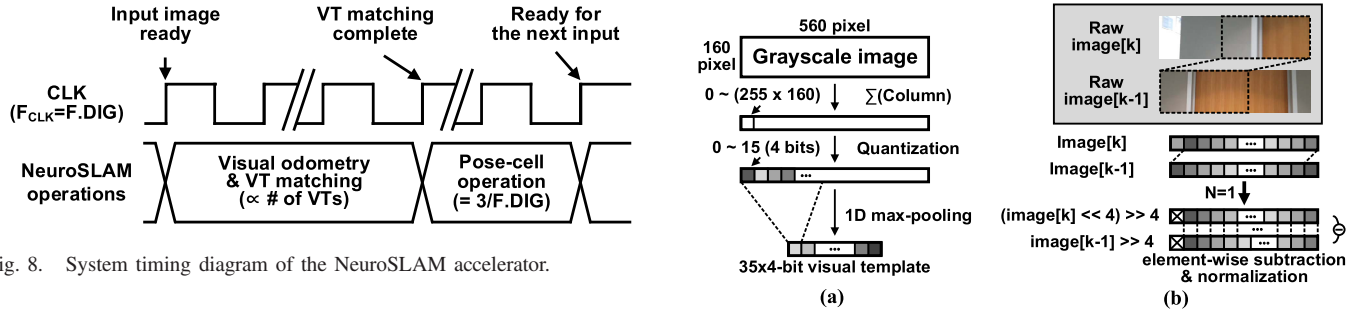


Fig. 8. System timing diagram of the NeuroSLAM accelerator.

odometry and the VT matching are performed. Since the VT matching requires a template scanning process, the processing time is proportional to the number of stored VTs in the SRAM. The pose-cell operations such as the energy shift and energy injection into a designated pose-cell are performed considering the results of the visual odometry and VT matching. The output of each process is fed to the off-chip experience map to compose a map. Each unit of the experience map consists of a matched VT index, a pose-cell address, and a position of the agent. The position of an agent in the unit is estimated by integrating the output of the visual odometry. It is worth noting that each process of the NeuroSLAM accelerator such as visual odometry, VT matching, the pose-cell operations, and the experience map management can be conducted in parallel via pipelining with necessary flag signals, even though the parallel operation is not illustrated in Fig. 8 for simplicity. The latency from the pipeline stages is negligible since the latency of the NeuroSLAM accelerator is dominantly determined by the VT scan. Fig. 9 shows the format of the image in the VT and a simplified diagram of visual odometry. The vision system of the NeuroSLAM accelerator relies on 140-bit scan-line intensity profiles where pixel-data are column-wise added, 4-bit quantized, and 1-D-max-pooled. The max-pooled input image provides the tolerance of image distortion on the NeuroSLAM to an extent. Compared to RatSLAM which employed three different raw images in the visual odometry and VT matching, the NeuroSLAM accelerator employs a single raw image that is used in VT matching (similar to RatSLAM) to compose a

Fig. 9. (a) Format of the image in the VT and (b) visual odometry.

140-bit 1-D input image and performs visual odometry and VT matching. There is a tradeoff between image compression and the accuracy of the SLAM results. While 1-D-max-pooling and quantization attain low power consumption with a  $64\times$  reduction in the memory footprint, the error in the visual odometry and the probability of false VT matches can increase. In this work, the parameter of the max-pooling and quantization is carefully set at the design phase, to achieve target SLAM accuracy in addition to increased power-and-area efficiency. The visual odometry extracts 4-bit translational velocity ( $v$ ) based on the difference between the current and the previous input image, and 4-bit rotational velocity ( $\omega$ ) estimated by the shifting index that leads to the minimum photometric error between the two images. Thereafter, path integration is initiated by accumulating the output of the visual odometry. Fig. 10 shows the path integration and the virtual pose-cell shift in the pose-cell controller. The digital head direction cell accumulates the rotational velocity and determines the current head direction of the agent. The head direction ( $\theta$ ) is quantized to a 2-bit resolution to represent the pose-cell energy shift. The pose-cell energy shift is initiated by accumulating the translational velocity. In case the accumulated value of the translational velocity exceeds a threshold of the energy shift, the virtual pose-cell energy shift is performed considering the head direction of the agent. Compared to RatSLAM where

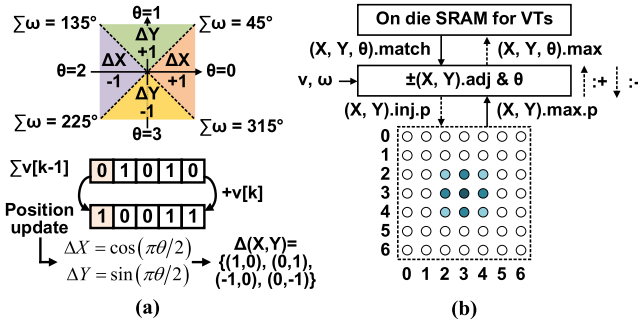


Fig. 10. (a) Path integration and (b) virtual pose-cell energy shift in the pose-cell controller.

fractional energy shift is conducted in every frame thereby incurring large power penalty, NeuroSLAM achieves power efficiency leveraging the integer shift of the pose-cell energy with the threshold. Furthermore, the virtual pose-cell shift is employed to avoid the shift of the actual energy in the pose-cell array. Since the energy in the pose-cell array is shifted by integer distances, it is power-efficient to rotate the address of the pose-cell array in view of the wrapping connectivity than to shift the actual energy in the pose-cell array. Thus, there is no actual energy shift in the pose-cell array during path integration. In order to mitigate the accumulated odometry errors during path integration, loop closure in the SLAM is tracked via VT matching where a new image needs to be compared to every stored VT. A VT consists of a 140-bit input image, the pose-cell address where the maximum excitation is located, and the 2-bit head direction when the VT is stored. A VT matching circuits determine whether an input image has been observed or not while employing parallel VT matching with dual thresholds and dynamic indexing to expedite the VT matching process. In case the input image is matched with a stored VT, energy is injected into the pose-cell and the digital head direction cell which are concatenated with the matched VT while considering the virtual pose-cell shift. Otherwise, a new VT is stored in the memory. When the VT match occurs and the maximum energy in the pose-cell array is located at the pose-cell address concatenated with the matched VT, loop closure occurs in the experience map where error correction leads to a redistribution of the distance error across the entire loop [28]. It is worth noting that there is no update on the pose-cell address retained in the SRAM during loop closure. The visual odometry generates a similar amount of deterministic errors while exploring the same path. The pose-cell addresses, which are generated during exploration of a previously-visited path, are the same as those stored during the first exploration. It helps avoid unnecessary energy injection and corresponding competition in the pose-cell array while retrieving the updated position of an agent from the experience map.

#### IV. IMPLEMENTATION OF THE NEUROSLAM FRONT-END

The NeuroSLAM accelerator achieves the power-efficient bio-inspired SLAM operations while implementing a hardware-friendly front-end. The 1-D-image-based visual odometry enables the NeuroSLAM accelerator to achieve the low-power self-motion estimation for edge devices.

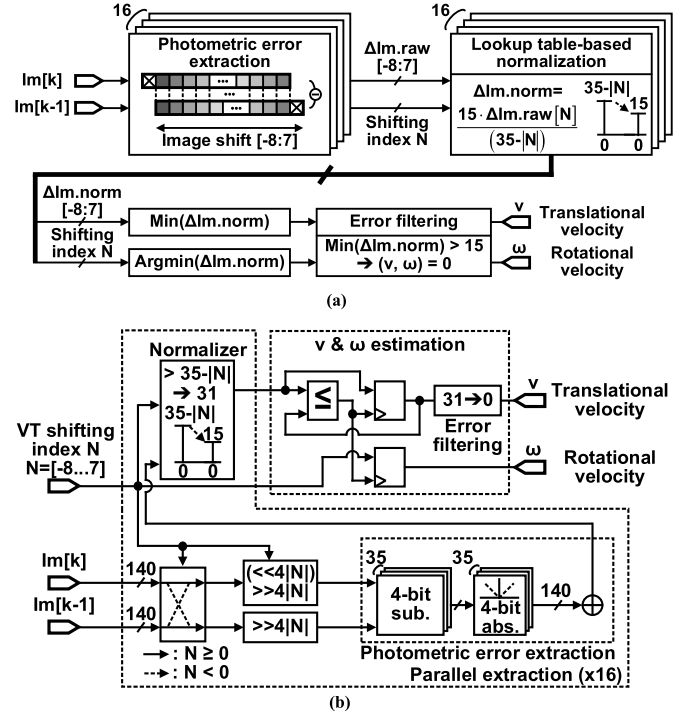


Fig. 11. (a) Functional diagram and (b) block diagram of the visual odometry.

Furthermore, the VT matching circuits with parallel and dual-threshold VT matching, and dynamic indexing expedite the template scanning process while reducing the number of memory access.

#### A. Visual Odometry

Fig. 11 shows the functional and block diagram of the visual odometry system. The visual odometry extracts the 4-bit translational and rotational velocity with 140-bit input images. The translational velocity is estimated by the photometric error of two consecutive images. The rotational velocity is estimated by the shifting index that the lowest photometric error occurs between two consecutive input images because the rotation of the agent exhibits a bitwise shift of the input image. Since the input image consists of 35 elements with 4-bit quantized grayscale image, the visual odometry shifts the image in the unit of 4 bits. The photometric error for each shifting index is extracted in parallel. Considering the shifting index, the number of elements used in extracting the photometric error varies from 27 ( $= 35 - |8|$ ) to 35. Thus, the normalization of the photometric error is employed to compare the photometric error considering the number of elements. In the normalization of the photometric error, a lookup table is used to avoid division operations in the digital block. Then, the 4-bit minimum photometric error and its 4-bit signed shifting index are fed to path integration block as the translational and rotational velocity. In case the minimum photometric error is exceedingly large due to an abrupt change of the input image, the visual odometry ignores the result as an error. Since the NeuroSLAM is a 5-degrees of freedom (DOF) SLAM architecture, the tilt of a camera, roll in 6 DOF, may incur errors in extracting rotational velocity. The proposed visual

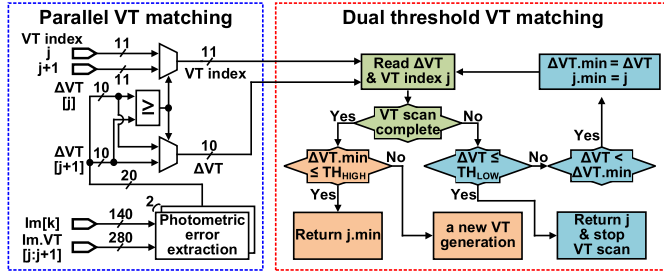


Fig. 12. Block diagram of the VT matching circuits.

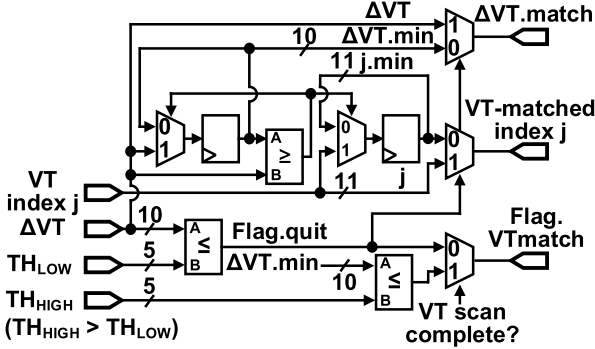


Fig. 13. Block diagram of the dual-threshold VT matching circuit.

odometry can extract rotational velocity unless a camera is severely tilted. We empirically determine that the camera can tolerate about  $6^\circ$  of tilt error, considering the aspect ratio of each section of 1-D-max-pooling.

### B. Visual Template Matching Circuits

The VT matching circuits minimize power consumption and latency via parallel and dual-threshold VT matching, and dynamic indexing. Fig. 12 illustrates the parallel and dual-threshold VT matching. The parallel VT matching is employed to expedite the VT matching. The parallel VT matching circuit extracts the photometric error ( $\Delta VT$ ) between the input VT and two stored VTs simultaneously. Then, the lower photometric error and its VT index are fed to the dual-threshold VT matching circuit. The dual-threshold VT matching controls the template scanning process based on the photometric error. Fig. 13 shows the block diagram of the dual-threshold VT matching circuit. In case an input image is matched with a VT with a lower difference than the low VT matching threshold ( $TH_{LOW}$ ), the template scanning process is immediately halted and the matched VT is returned while reducing further memory access. Otherwise, the full scan of the VT is conducted. Then, the VT matching circuits determine whether a new VT should be generated or not. In case the minimum photometric error during the full VT scan exceeds a high VT matching threshold ( $TH_{HIGH}$ ), a new VT is appended, thus reducing the total memory usage compared to employing a single threshold  $TH_{LOW}$ . If  $TH_{LOW} < \Delta VT < TH_{HIGH}$  for every VT, the best matched VT index is returned with a full scan of stored VTs. During template matching, the dynamic indexing is also exploited to shorten the scanning process. Fig. 14 depicts the dynamic indexing during the VT

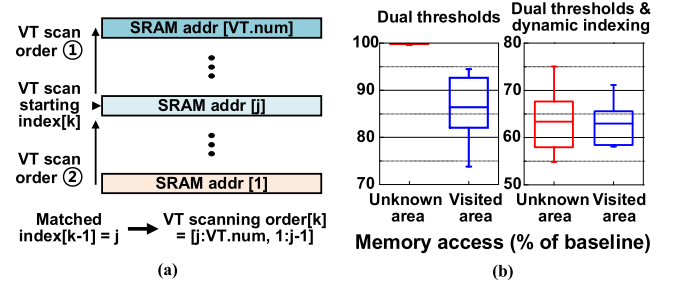


Fig. 14. (a) Dynamic indexing in the template matching and (b) simulation results of the memory access with the dual thresholds and dynamic indexing.

scan and its simulation results. Since a VT is stored in the SRAM sequentially, the vicinity of the last matched VT may contain a similar image to the next input. We exploit the fact that once the agent observes a previously seen visual cue (i.e., VT match at index  $[j]$ ), the probability of a VT match for the next input is high near the index  $[j]$ , by starting the VT search at the index  $[j]$ . The simulation results of the memory access compared to the baseline without dual thresholds and dynamic indexing are shown in Fig. 14. The dual thresholds and dynamic indexing enable the NeuroSLAM to reduce the number of memory accesses to 63% of the baseline. In particular, the dynamic indexing is efficient while exploring an unknown area. Since the probability that a newly generated VT is likely to match with the next input, it can dramatically shorten the scanning process.

It is noteworthy that there is no global reallocation of VTs in the SRAM for each visited scene. Instead, multiple local VT groups for certain scenes are composed when an agent explores a certain area multiple times, since VTs are stored sequentially. Alternatively, we can also employ a global reallocation of VT. If we do use a global reallocation policy, the probability that the immediate VT match occurs increases since all the images stored at a certain scene are placed in the vicinity of a certain index. However, the overhead in sorting VTs is inevitable. In particular, the overhead may hinder an agent from supporting online SLAM since a continuous sorting of VTs is required. From our simulations and empirical results, we note that local VT groups provide an effective tradeoff, reducing the total number of memory accesses without any requirement of global sorting.

## V. MIXED-SIGNAL OSCILLATOR-BASED POSE-CELL ARRAY

Localization in the NeuroSLAM accelerator is performed through a bio-mimetic  $7 \times 7$  SNN-based pose-cell array. An oscillator-based pose-cell represents the energy of the pose-cell as the frequency of the oscillator. Each pose-cell is connected with adjacent pose-cells and exhibits the dynamics of continuous attractor networks (CANs).

### A. CANs in the Pose-Cell Array

A CAN is a well-known model to mimic the behavior of place cells and other neural activities [30]. A CAN has an array of units of a neural model with weighted connections. The



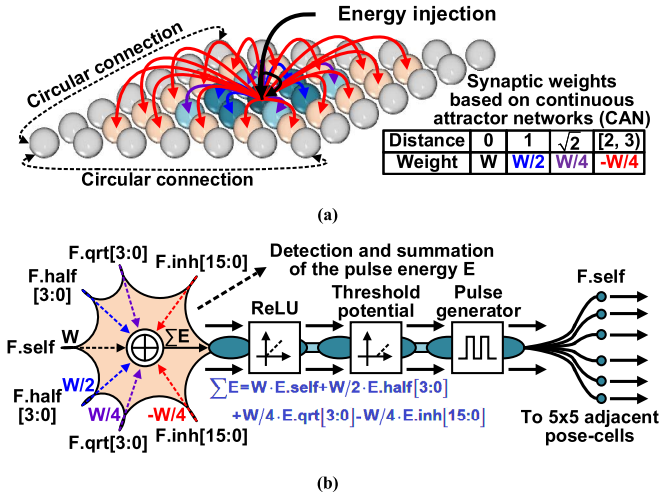


Fig. 15. (a) CAN in the pose-cell array and (b) functional diagram of the oscillator-based pose-cell.

neural unit in CANs performs MAC operations considering the energy of adjacent units and the weight. The main feature of CANs is that the connection is recurrent. The recurrent connections lead to continuous-time operations in CANs and result in convergence. The weight of the connections is modeled by the Mexican hat wavelet [31], the negative normalized second derivative of a Gaussian function. Owing to excitatory and inhibitory connections in CANs, a group of excited units, called an attractor, exists in a converged state, and each attractor competes against the other attractors. Fig. 15 shows the connections in the pose-cell array and the functional diagram of the oscillator-based pose-cell. The pose-cell array employs CANs to mimic place cells. Each pose-cell has excitatory and inhibitory connections to its neighbors with distance-dependent weights and circular boundary conditions to enable continuous tracking while preventing the size of the map from exploding. The weight distributes the energy to adjacent pose-cells and it composes a group of excited pose-cells as an attractor in the pose-cell array. Each attractor competes against the other attractors due to the negative weight for distant pose-cells. In each pose-cell, the energy from adjacent pose-cells is accumulated as a control voltage of the oscillator scaled by the corresponding weight. Since the lower limit of the control voltage is ground, the pose-cell has an inherent characteristic of a rectified linear unit (ReLU). In addition, the threshold of the oscillator is used to maintain sparse energy distribution in the pose-cell array by preventing insignificant energy from incurring spurious oscillations in the pose-cell. Then, considering the control voltage, the pulse for the next state is generated and distributed to adjacent pose-cells.

### B. SNN-Based Pose-Cell

Fig. 16 illustrates the block diagram of the oscillator-based pose-cell. Each pose-cell features a five-stage ring voltage-controlled oscillator (VCO) to implement rate-coded spiking neurons, 4-bit current DACs (IDACs) for each excitatory and inhibitory connections, global inhibition and current

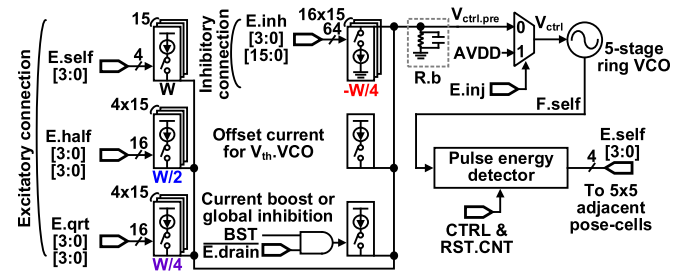


Fig. 16. Block diagram of the oscillator-based pose-cell.

boost (BST), and a 4-bit asynchronous counter (CNT)-based pulse energy detector that encodes the pose-cell energy. The offset current in the pose-cell is employed to adjust the dead zone of the pose-cell caused by the threshold voltage of the VCO. The dead zone suppresses the oscillation due to insignificant energy at the pose-cell and significantly reducing the total pose-cell array energy. The frequency of excited pose-cell is proportional to the amount of its energy content. The global inhibition and current BST assist the competition of the attractors and the preservation of the energy distribution in the pose-cell array, respectively. Since the total energy in the CAN should be normalized to prevent the depletion or the saturation of energy, RatSLAM conducts the normalization in digitally within the digital pose-cell. In order to avoid extremely high dynamic range of computation, such as summations and divisions of the energy of the entire network, the NeuroSLAM employs current BST to preserve significant energy without the normalization. The weight in the pose-cell array is set to gradually attenuate the energy of the attractors, which is the global inhibition. In case the energy of the pose-cell exceeds a certain threshold, the current BST is asserted to inject additional energy into the pose-cell, thereby preserving the attractor in the pose-cell array while suppressing other pose-cells that carry insignificant energy. A pulse energy detector is employed at the end of the pose-cell to convert the energy of the pose-cell, i.e., the frequency of the VCO, to a 4-bit digital signal. Compared to the functional diagram where the pose-cell directly distributes the pulse to adjacent pose-cells shown in Fig. 15, in the circuit implementation, the energy is distributed in the form of 4-bit digital signals via the pulse energy detector. If the pulse is directly fed to 25 adjacent pose-cells, the 25 pulse energy detectors are necessary in each pose-cell and it leads to prohibitive power-and-area inefficiency. Thus, the pose-cell distributes the energy of the pose-cell in a 4-bit digital signal while achieving bio-mimetic spiking operations in each pose-cell. It is worth noting that the proposed mixed-signal pose-cell array achieves high energy efficiency while demonstrating the bio-mimetic characteristic of CANs and SNNs with analog spiking signals. The absence of any global clock allows the system to scale, while the sparse switching of SNNs enables low power dissipation.

Fig. 17 depicts the schematics of the IDAC, the VCO, and the pulse energy detector in the pose-cell. Each pose-cell comprises 25 4-bit IDACs and a resistive load to accumulate the energy from 25 adjacent pose-cells scaled by the weights. The pose-cell contains 9 sourcing and 16 sinking IDACs for

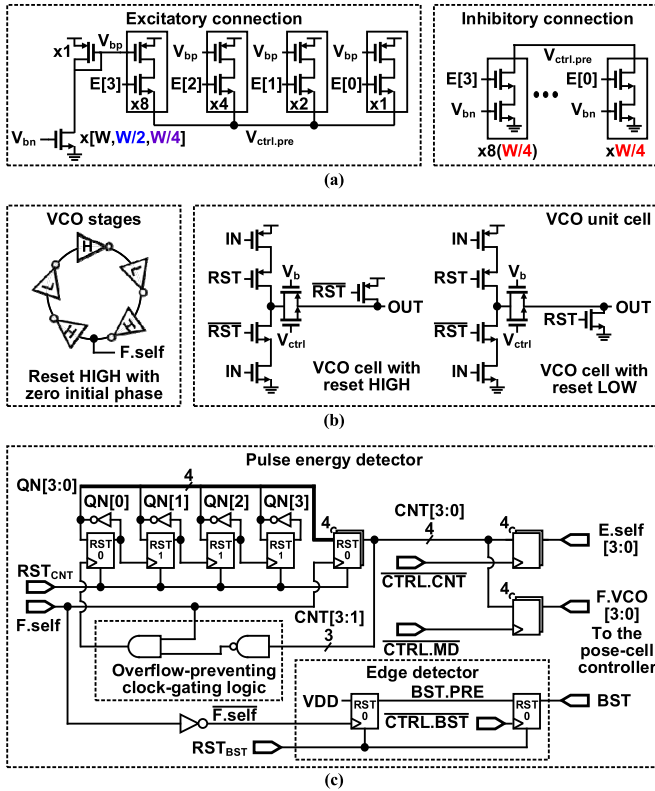


Fig. 17. Schematics of (a) current DAC, (b) VCO, and (c) pulse energy detector in the pose-cell.

excitatory and inhibitory connections, respectively. The weight of each connection is determined by the unit current of the IDAC. The output current of each IDAC representing the multiplication of the 4-bit input energy by the unit current is accumulated at the node with the resistive load and converted to the voltage ( $V_{ctrl,pre}$ ) as the final output of the mixed-signal MAC operation. The VCO generates the frequency proportional to the aggregate energy of each pose-cell. Since the frequency of the VCO is converted to the 4-bit digital energy via the CNT-based pulse energy detector, the phase reset of the VCO is important to estimate the accurate energy of the pose-cell. Thus, the VCO clock signal is reset to zero phase considering the reset polarity of each VCO stage. Furthermore, the VCO employs a pseudo-NMOS transmission gate to linearize the output frequency over the range of control voltages with the bias voltage of the PMOS gate ( $V_b$ ) [32]. In the pulse energy detector, the rising edges of the VCO clock signal ( $F_{self}$ ) are counted during 16 periods of the VCO clock signal that oscillates at the maximum frequency ( $F_{max}$ ). Since the pulse energy detector is based on the 4-bit clock CNT, a clock-gating logic is employed to prevent the overflow of the CNT in case the VCO oscillates at the maximum frequency. The pulse energy detector uses D flip-flops (DFFs) to sample the output of the CNT. Fig. 18 shows the flowchart and the timing diagram of the pose-cell operation. The pose-cell array has three states called the CNT, BST, and max detection (MD) state in addition to the operations of the energy injection and drain considering the VT match. In case the input VT is not matched with the stored VTs, the flag of the energy injection ( $E_{inj}$ ) and the energy drain ( $E_{drain}$ ) is not asserted in the

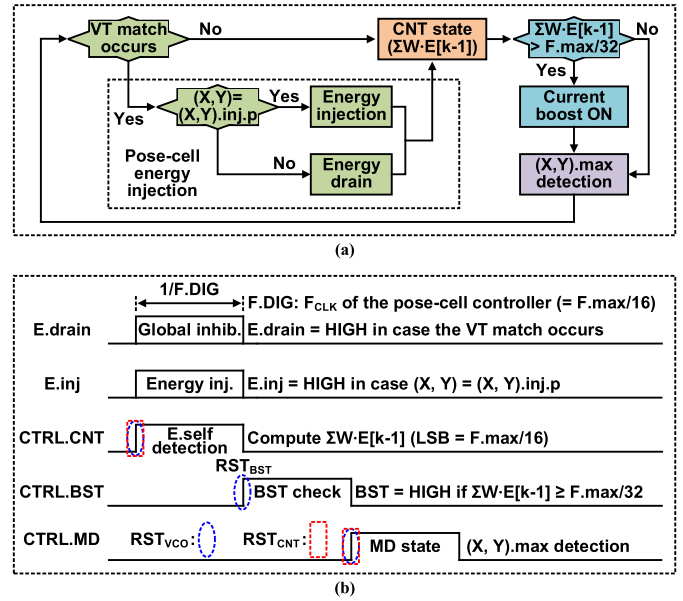


Fig. 18. (a) Flowchart and (b) timing diagram of the pose-cell operation.

CNT state. At the beginning of the CNT state, the energy in the previous frame ( $E[k-1]$ ) from adjacent pose-cells is fed to the IDAC-based MAC accelerator. The VCO generates the frequency considering the aggregate energy ( $\Sigma W \cdot E[k-1]$ ). The 4-bit clock CNT in the pulse energy detector is reset to estimate the frequency representing the aggregate energy. During this state, the current BST in each pose-cell is asserted based on the energy in the previous frame. At the end of the CNT state, the pulse energy detector samples the output of the 4-bit CNT using the DFF with the control signal of the CNT state ( $CTRL.CNT$ ) as the 4-bit energy ( $E_{self}[3:0]$ ). In the BST state, each pose-cell evaluates whether the pose-cell obtains the energy worth contributing to compose the attractor. The BST state uses the edge detector in the pulse energy detector. At the beginning of the BST state, the VCO and the edge detector are reset. Since the output of the VCO is reset to the supply voltage with zero phase, the input of the edge detector is set to ground at the reset. The output of the first DFF ( $BST.PRE$ ) is asserted when a rising edge occurs at the clock signal. At the end of the BST state, the second DFF samples the data as the control signal of the current BST. Considering the fact that the rising edge occurs after a half period of the VCO clock signal, the threshold of the current BST is the 1/32 of the maximum frequency of the VCO. Then, the control signal of the current BST is updated for the energy in the current frame ( $E[k]$ ) and the VCO in the pose-cell array oscillates considering the energy. In the MD state, the energy of the pose-cell is estimated to detect the address of the pose-cell that has the maximum energy in the current frame. The VCO and the 4-bit CNT are reset at the beginning of the MD state. The output of the CNT is sampled by the DFF with the control signal of the MD state ( $CTRL.MD$ ) as the 4-bit energy for the pose-cell controller ( $F.VCO[3:0]$ ). Then, the pose-cell controller retrieves the pose-cell address where the maximum excitation is located for further operations such as a new VT generation and loop closure.



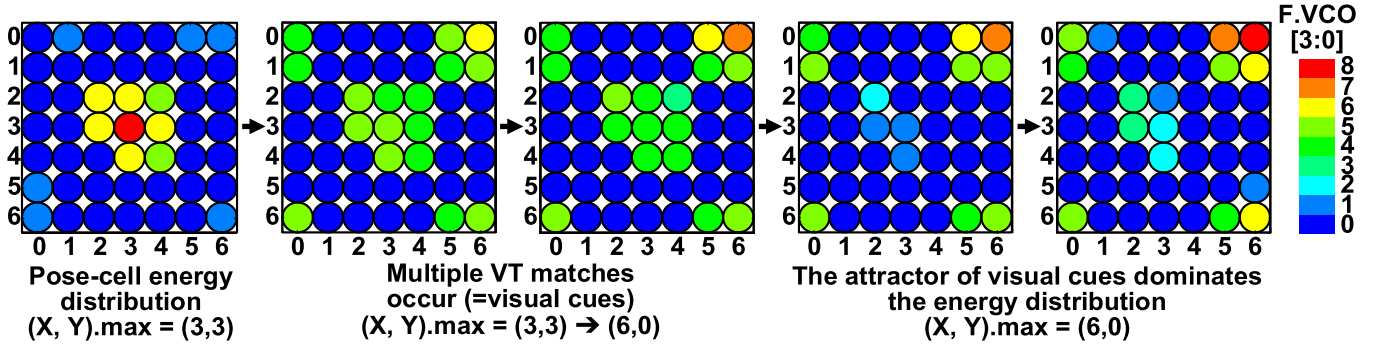


Fig. 19. Measured pose-cell activities in the pose-cell array.

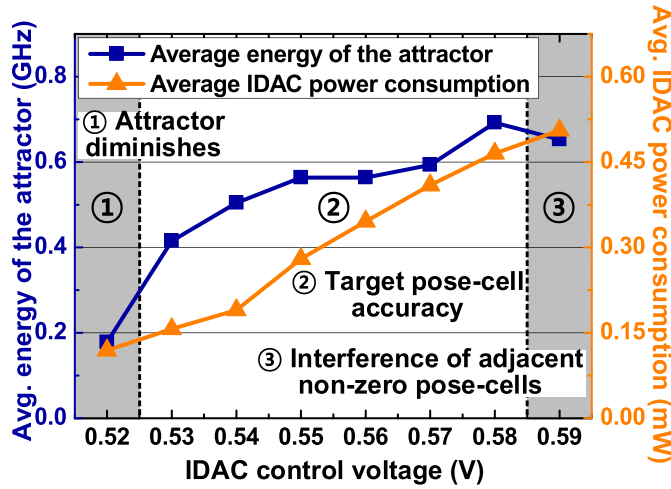


Fig. 20. Measured pose-cell operation region over the current DAC control voltages.

When a VT match occurs at the NeuroSLAM front-end, the pose-cell controller injects energy into the corresponding pose-cell address concatenated with the matched VT. In this case, the flag of the energy injection and the energy drain is asserted during the CNT state. The flag of the energy injection is asserted only for the designated pose-cell considering the virtual pose-cell shift. Since the flag sets the control voltage of the VCO to the supply voltage, the VCO of the designated pose-cell generates the maximum frequency during the CNT state. Then, the energy is distributed to adjacent pose-cells and this generates a new attractor in the pose-cell array. For the other cells, the flag of the energy drain is asserted to deactivate the current BST. It initiates a competition between the attractor of the self-motion cues and a new attractor by lessening the total energy of the existing attractor.

It is noteworthy that the size of the pose-cell array is optimized considering the dimension of the environment that the agent explores and the probability that a false VT match occurs. Since the pose-cell array employs the wrapping connectivity to encompass a vast environment, the VTs created at different locations have the probability to contain the same pose-cell address. In case the pose-cell address concatenated with the falsely matched VT is the same as the current pose-cell address that has the maximum excitation in the pose-cell array, a false loop closure occurs and the accuracy of the

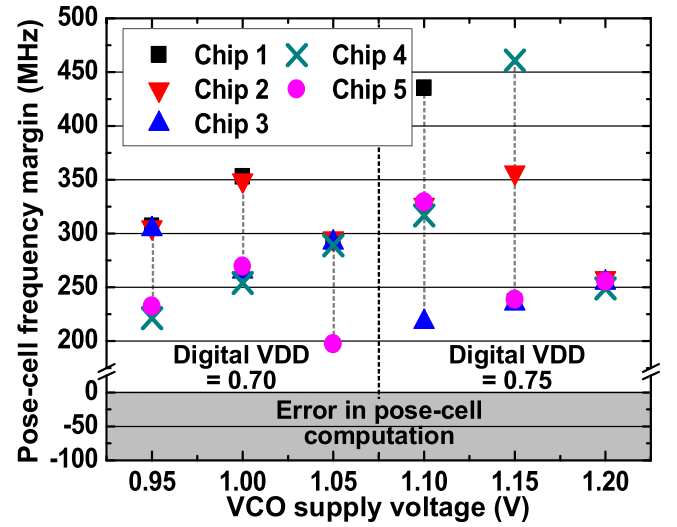


Fig. 21. Measured pose-cell frequency margin in the pose-cell operation.

SLAM result is affected. Thus, there is a tradeoff between the area due to the dimension of the pose-cell array and the probability of a false loop closure. In this work, we set the size of the pose-cell array based on models of indoor environments which is our domain of interest.

## VI. MEASUREMENT RESULTS

The proposed NeuroSLAM accelerator IC is fabricated in a 65-nm CMOS process and assembled in a QFN48 package. The test chip allows the agent to continuously move and acquire data, and the map is seamlessly updated, corrected, and appended. Due to the limited speed of a serial camera-interface in the current design, the NeuroSLAM operates at 10 frames per second (fps) as the same as RatSLAM. However, the NeuroSLAM architecture itself can support >100 fps. Fig. 19 illustrates the measured pose-cell activities over frames in the pose-cell array. Each pose-cell can be stalled in its current state and the corresponding energy can be individually readout to provide unique observability into SNN attractor dynamics. The pose-cell activities demonstrate one instance of the measured competition of the  $7 \times 7$  array where the attractor of the self-motion cues is initially placed at (3,3). After a VT match, a new visual cue injects energy into (6,0). Owing to the nature of the CAN, the injected energy composes a new attractor.

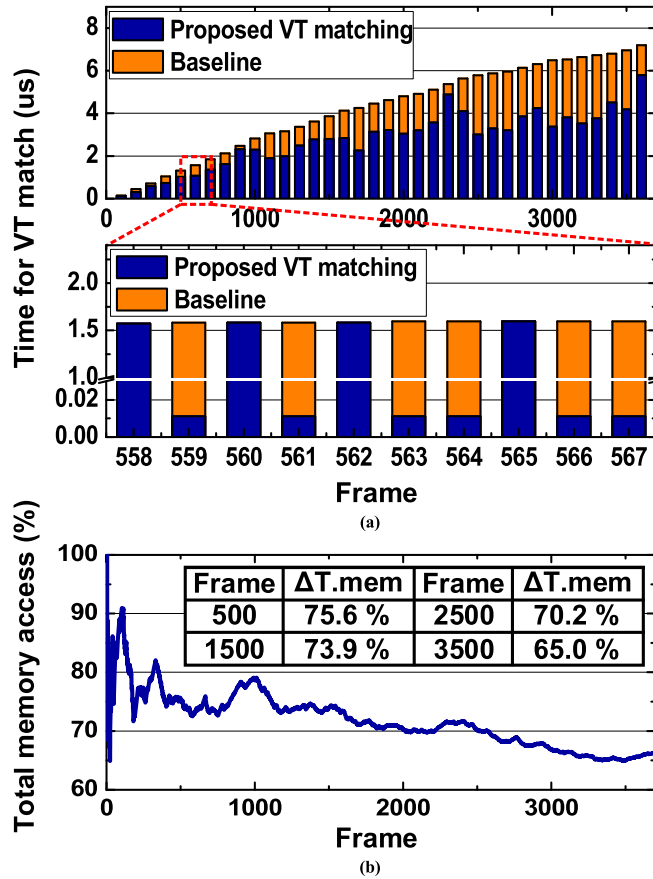


Fig. 22. (a) Measured memory access and (b) measured total memory access compared to the baseline over frames.

With multiple VT matches, a new attractor obtains more energy and starts to suppress the attractor of the self-motion cues. Finally, the neuronal dynamics eventually corrects the error accumulated due to the visual odometry. Fig. 20 shows the measured pose-cell operation region over IDAC control voltages. The IDAC control voltage is tuned to provide a robust attractor ( $> 500$  MHz of pose-cell firing rate) while minimizing spurious spiking by non-excited pose-cells and reducing the power consumption. In case the current in the pose-cell array is low, an attractor automatically diminishes in the pose-cell array. In the appropriate current range, an attractor exists stably in the pose-cell array. In case the current is excessively high, a sparse energy distribution cannot be maintained and spurious oscillations can occur thereby affecting the correct operation of the pose-cell operation. Fig. 21 shows the measured pose-cell frequency margin in the pose-cell operation. Mismatches and random process variation among the pose-cell VCOs can cause certain pose-cells that have a lower threshold voltage of the VCO to fire spuriously even when they are weakly excited. In the worst case, a spurious pose-cell can fire faster than the pose-cell with the maximum excitation and can incur algorithmic errors. We quantify the robustness of the system as the pose-cell frequency margin (= frequency of pose-cell with maximum excitation – worst case spurious firing) and show measurements across multiple dies illustrating the frequency margin of 200 MHz with correct operations

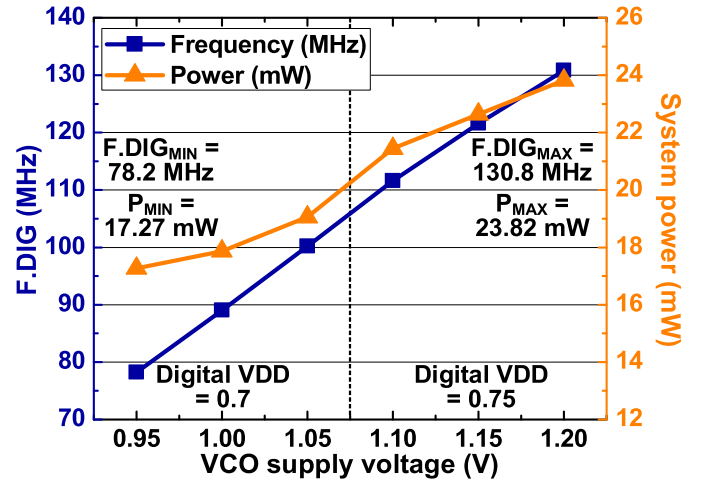


Fig. 23. Measured operating frequency and power consumption of the NeuroSLAM accelerator.

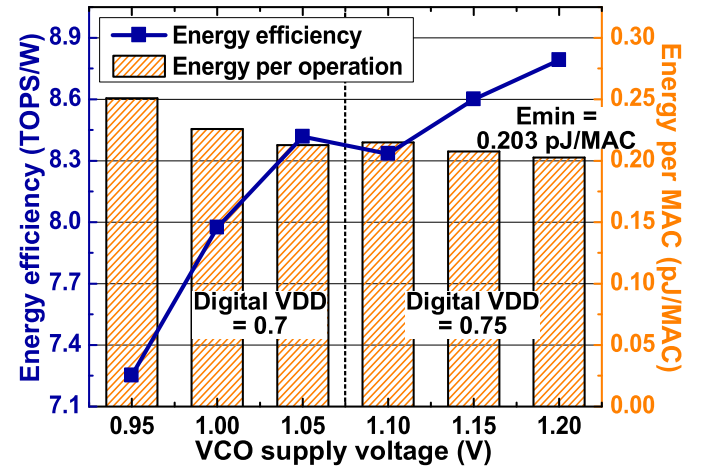


Fig. 24. Measured energy efficiency and energy per MAC operation over supply voltages of the VCO in the pose-cell array.

across the entire operating range. Fig. 22 shows the measured memory access during the VT matching. Owing to the dual thresholds and dynamic indexing in the template matching, the number of memory access is dramatically reduced over frames. In particular, the VT matching completes with only a single memory access in many frames owing to dynamic indexing. The latency of the VT matching scheme is reduced to 65% compared to the baseline that does not employ the dual thresholds and dynamic indexing. Fig. 23 shows the measured operating frequency and power consumption of the NeuroSLAM accelerator. Over the supply voltage of the VCO in the pose-cell array, the pose-cell controller operates at the frequency of 78–130 MHz. The power consumption of the test chip is 17.27–23.82 mW under the 4-bit SNN-based pose-cell operation. Fig. 24 shows the measured energy efficiency and energy per MAC operation. The energy efficiency of 7.25–8.79 TOPS/W is achieved. Furthermore, the test chip achieves 0.203 pJ/MAC. It is worth noting that the energy efficiency increases over the supply voltages of the VCO. Compared to digital MAC accelerators where the energy-efficiency typically decreases in the super-threshold region [33], the mixed-signal

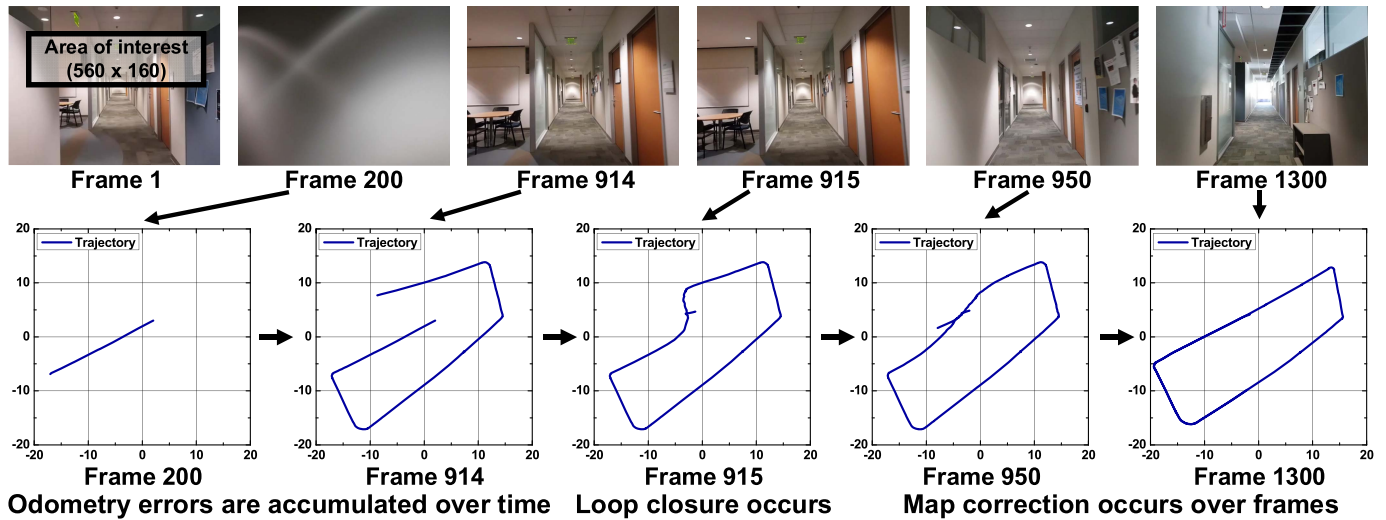


Fig. 25. Measured experience map over frames with the first loop closure.

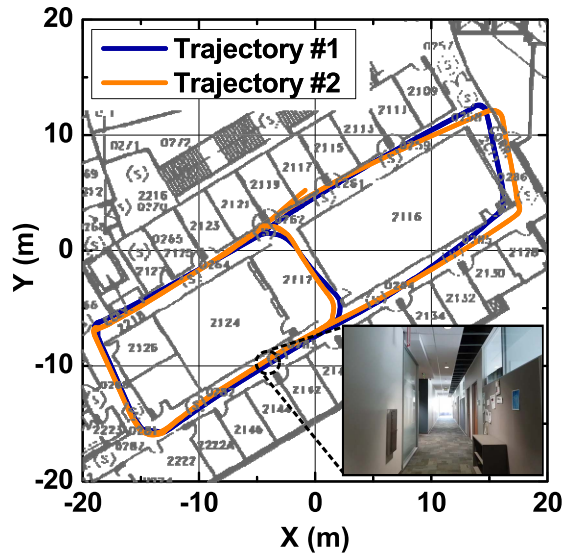


Fig. 26. Measured SLAM results of the NeuroSLAM accelerator.

oscillator-based NeuroSLAM accelerator operates more efficiently over high supply voltages. That means that the NeuroSLAM accelerator is more efficient when higher throughput is required. Fig. 25 illustrates the measured experience map over frames with the first loop closure during a typical SLAM operation. The odometry errors are accumulated during path integration. Once the agent visits a previously explored area, loop closure occurs and the accumulated error is corrected over frames by redistributing the distance error across the entire loop. Fig. 26 shows the measured SLAM results of the NeuroSLAM accelerator. The final SLAM results are obtained by the experience map management inherited from RatSLAM [28]. Considering the superimposed blueprint of the area, the NeuroSLAM successfully demonstrates the SLAM operation with loop closure. The NeuroSLAM accelerator composes a hybrid of metric and topological maps similar to RatSLAM, while using relative coordinates. Compared to metric maps [11], [18], topological maps primarily give

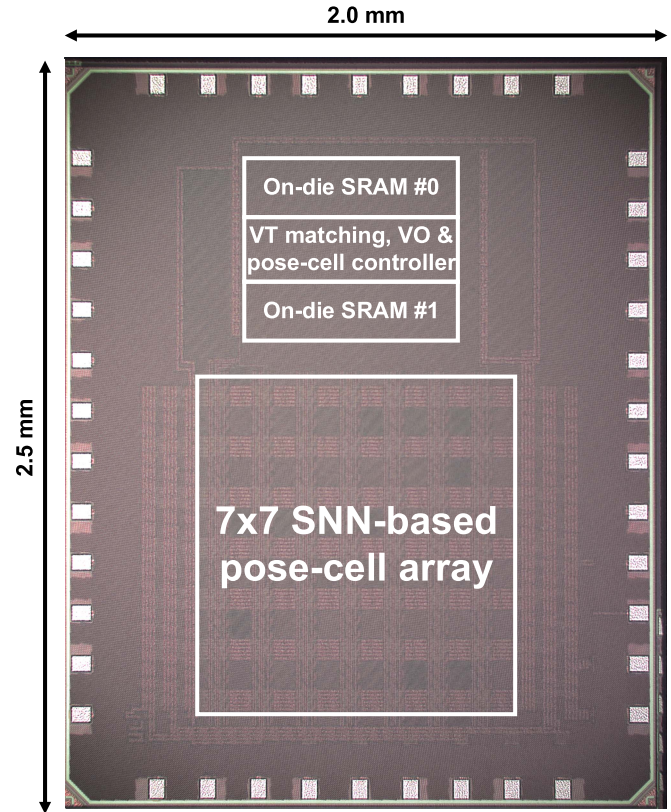


Fig. 27. Microphotograph of the test chip.

importance to junctions of a path, i.e., loop closure, rather than the local accuracy of each position of an agent. The estimated root mean square (rms) error of the SLAM results is 0.437 m. Considering that the estimated rms error with the original RatSLAM algorithm is 0.370 m, the NeuroSLAM accelerator achieves the appropriate metric accuracy and energy efficiency with a  $64\times$  reduction in the memory footprint under no false loop closure. Furthermore, since we assume that the agent generates and uses its own map, deterministic metric errors



TABLE I  
SYSTEM SUMMARY AND COMPARISON

		TVLSI 2013 [1]	JSSC 2015 [2]	JSSC 2019 [11]	ISSCC 2019 [18]	This work
System	Type	Pose estimation	Pose estimation	SLAM	SLAM	SLAM
	DOF	6-DOF	6-DOF	6-DOF	6-DOF	5-DOF
	Front-end	Marker based	SIFT	Harris	CNN	Direct method with maxpooling
	Back-end	N/A	N/A	Keyframe-based	Keyframe-based	NeuroSLAM
	Odometry	Visual odometry	Visual odometry	Inertial sensor	Visual odometry	Visual odometry
	Map type	Not specified	Not specified	Metric	Metric	Metric & topological
Technology		180 nm	65 nm	65 nm	28 nm	65 nm
Supply voltage		1.8 V	1.2 V	1.2 V	0.63-0.9 V	0.7-0.75 V (Digital) / 0.95-1.2 V (Analog)
Design		Digital	Digital	Digital	Digital	Mixed-signal
Frequency		200 MHz / 100 MHz	133 MHz	62.5 MHz / 83.3 MHz	240 MHz	78.2-130.8 MHz
Resolution		640 x 480	640 x 480	752 x 480	640 x 480	640 x 480
On-chip memory		N/A	96 kB	854 kB	1126 kB	37.9 kB
Performance		153.6 GOPS	20.2 GOPS	10.5-59.1 GOPS	879.6 GOPS @ 0.9 V 329.8 GOPS @ 0.63 V	142.49 GOPS @ 1.0 V 209.41 GOPS @ 1.2 V
Power		413 mW	27 mW	24 mW	243.6 mW @ 0.9 V 61.75 mW @ 0.63 V	17.87 mW @ 1.0 V 23.82 mW @ 1.2 V
Energy efficiency		0.37 TOPS/W	0.75 TOPS/W	0.43-2.5 TOPS/W	3.6 TOPS/W @ 0.9 V 5.34 TOPS/W @ 0.63 V	8.0 TOPS/W @ 1.0 V 8.79 TOPS/W @ 1.2 V
Area		28.75 mm <sup>2</sup>	3.25 mm <sup>2</sup>	20 mm <sup>2</sup>	10.92 mm <sup>2</sup>	5 mm <sup>2</sup>
Application		AR and VR		High performance AR, VR, and UAVs		Ultra low power microrobotics [edge AI]

\* 1 MAC = 2 OPS

dominantly caused by the visual odometry has less impact on the exploration of the agent while using its own map. Fig. 27 shows the microphotograph of the test chip. Table I summarizes and compares the SLAM performance with existing solutions. In the comparison table, we have compared the current design with other SLAM-based ASICs. Prior designs that target SNNs allow programmable connectivity and target a completely different application space; and hence they are not included in Table I. The comparison table shows competitive figures-of-merit, ultra-low power operation, and successful system integration and deployment. An asynchronous/event-based digital design is estimated to operate at the same equivalent energy/power-levels for processing each frame. However, such a digital implementation cannot achieve a neural spiking model demonstrating actually spiking signals. The test chip is the first bio-inspired SLAM IC with a lightweight vision system for applications in edge robotics. Since power consumption is a hard constraint in edge devices, the NeuroSLAM achieves target accuracy and throughput while meeting stringent power constraints.

## VII. CONCLUSION

This article presents a 7.25-to-8.79-TOPS/W mixed-signal oscillator-based NeuroSLAM accelerator for applications in edge robotics. SLAM is a quintessential problem in autonomous navigation, augmented reality, virtual reality, etc. Furthermore, SLAM at edge devices has come into the limelight with the emergence of edge intelligence. In particular, ultra-low power SLAM systems are of importance for applications in edge robotics due to battery-powered edge devices. The design presented in this article satisfies the strict criterion on power consumption for edge devices by incorporating a bio-inspired SLAM architecture with the lightweight vision system while achieving appropriate SLAM results.

The proposed NeuroSLAM accelerator IC achieves ultra-low power consumption employing a mixed-signal oscillator-based pose-cell array and the 1-D-image-based vision system. The pose-cell array and the digital head direction cell are employed to mimic place cells and head direction cells in a rodent brain. Furthermore, a CAN with the wrapping connectivity is implemented in the pose-cell array to mimic the principles of spatial cognition in rodents, while achieving a sparse energy distribution and the continuous tracking capability. The lightweight vision system with a max-pooling supports low-power visual odometry and re-localization. The NeuroSLAM accelerator IC demonstrates correct SLAM operations and successful loop closure. The test chip fabricated in a 65-nm CMOS exhibits a peak energy efficiency of 8.79 TOPS/W with a power consumption of 23.82 mW.

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