Modeling and Analysis of System Stability in a Distributed Power Delivery Network with Embedded Digital Linear Regulators

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Abstract – On-chip power delivery networks (PDNs) for today's microprocessors and systems-on-chip (SoCs), which are characterized by dynamic supply voltage, many embedded integrated VRs (IVRs), lower decoupling-capacitor, high current ranges, multiple power modes and fast transient loads are designed to minimize AC load transients and supply noise. The close interaction of the VRs with the power grids create multiple feedback paths in the overall network, compromising the resultant phase margin and can even lead to system instabilities. The introduction of digital linear regulators operating in the low dropout (LDO) mode, with low power supply rejection, further exacerbates the problem. This paper provides a comprehensive methodology, based on Mason's Gain Formula applied to hybrid control, for modeling and analyzing distributed linear regulators and their interaction with the PDN.

I. INTRODUCTION

Microprocessors and SoCs continue to improve both performance and power efficiencies with technology scaling extending beyond 22nm. Multiple voltage islands provide fine-grained spatial and temporal control of the operating voltage and frequency, and software controlled power-states enable low standby power along with fast wake-up enabling digital circuits to expand their dynamic ranges of operation. The integration of on-die Voltage Regulation on the core microprocessor [1] allows faster and wider dynamic voltage and frequency scaling (DVFS). Finer regulation is achieved with voltage regulators designed in a hierarchical manner, e.g., off-die buck converters serving as the voltage regulator module (VRM) followed by switched capacitor (SC) VRs (either on or off-die) and on-die linear VRs. As shown in Fig. 1, they provide fine-grained spatiotemporal supply adjustments. Linear regulators operating in LDO mode can be designed with one regulator supplying power to a single grid or even multiple regulators supplying power to a single grid. The latter is an attractive design choice as it allows one or more regulators to be switched-off at light load, thereby increasing the overall system power efficiency. Unfortunately, fine-grained power management comes at the expense of lower de-coupling capacitor per grid, higher IR drops, and complex interconnected systems where the VRs interact with each other and the PDN, forming multiple feedback paths. In most cases this leads to over-design in which power efficiency and regulation granularity is sacrificed with increased guard bands. Linear voltage regulators (LVRs) [2-4] are widely used for local supply regulation with fast transient response. Analog design solutions are popularly used for LDOs but they do not integrate well with the digital design/process flow requiring custom integration and placement. Consequently, design solutions have been proposed for linear regulators with digital control using digital process and libraries. Such LDOs can be discrete time [2] or continuous time [3] with high efficiencies providing seamless process and design integration. Although digital regulators provide high efficiency, sufficient bandwidth and ease of integration, they do suffer from lower power supply rejection (PSR), thereby making them more prone to interactions with the PDN. With the popularity of digital LVRs, it is prudent to investigate not only the overall stability of such LVRs, but also understand how they interact with the PDN, when multiple VRs drive separate or common digital loads. This problem is exacerbated by the fact that digital loads undergo large dynamic ranges, resulting in significant movement of the output pole frequency, thereby making it difficult to guarantee overall system stability across the operating range. Further as digital LVRs suffer from lower PSR the overall PDN with distributed digital LVRs are more susceptible to instabilities or loss of margin. This calls for the development of compact models for distributed digital LVRs in an interacting PDN, which can provide designers with design tools and methods to analyze and optimize the gain, placement, sampling frequencies of digital LVRs, as well as guide the choice of de-caps, off-chip components and necessary supply guard-bands across chip power states.

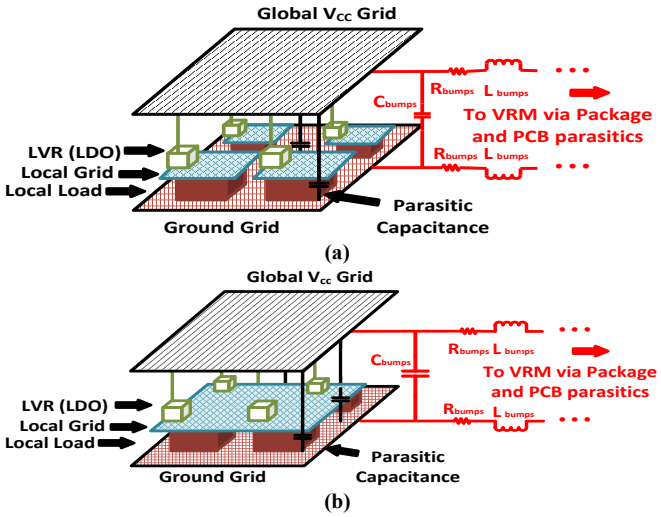


Fig. 1 (a) A multi-Vcc chip showing a power delivery network with local grids, LDOs driving each grid, the global Vcc grid and off-chip routing to the VRM (b) A multi-Vcc chip showing the LDOs with single local grid driven by multiple LDOs, the global Vcc grid and off-chip routing to the VRM.

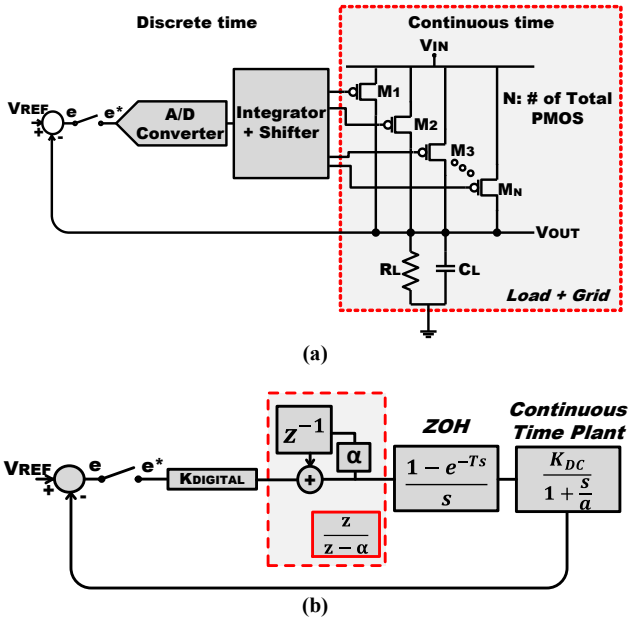


Fig. 2 (a) Block Diagram of a digital Linear Regulator (b) A control diagram illustrating the hybrid control.

Recently, a hybrid stability theory has been proposed in [5] which is used to analyze the stability of analog LDOs in a power grid by identifying passivity violations [6]. The methodology provides a fast evaluation of the system stability at discrete pre-determined frequencies but, for certain frequency ranges stability cannot be guaranteed. Further, the authors in [6-7] have proposed to find the finite gain characteristics of an analog LDO over a range in which a passive mapping no longer exists. However, the use of the hybrid passivity and finite gain theorem to control practical, yet sufficiently complicated plants has not yet been demonstrated. Further, digital LDOs with discrete time control pose additional challenges for modeling and analysis, since they represent a distributed and hybrid control system. Although the designs and models of analog LDOs are well understood [4-6], digital LDOs have been recently proposed for digital loads [2] and their control model has not been analyzed.

In this paper we provide a hybrid control model for digital discrete-time LDOs and investigate how distributed LDOs interact with themselves and the PDN simultaneously. Using a graph-theoretic approach for solving *Mason's Gain Formula* in a complex multi-LDO grid, we:

(a) Provide hybrid models for discrete time LDOs.

(b) Analyze the overall system stability that handles the continuous time PDN and the discrete time VR, and

(c) Provide performance and stability optimization criterion for multi LDO based PDN across the entire frequency range of interest.

II. ALL DIGITAL LDOs

Power management of microprocessors and SoCs contain both off-chip switching converters and on-chip LDOs to provide regulated power supplies to different voltage islands. For digital loads requiring large dynamic range, the impetus for a local LDO are digital design, fine spatio-temporal voltage regulation and higher system power efficiency. This often comes at an expense of reduced PSR, higher output ripple (due to limit cycle oscillations in digital control) and lower loop bandwidth. The discrete-time, digital LDO proposed in [2] consists of two main stages: an ADC input stage, and a current based -DAC at its output stage. As shown in Fig. 2a, the ADC samples the output voltage at the rising edge of the ADC clock. In its simplest implementation, the ADC can be just a 1-bit comparator that determines if the output voltage is greater or lower than the reference voltage. The ADC output will provide a digital word that measures the separation of the output voltage from the reference. This code-word is used in the control loop to turn on or turn off power MOSFETs through a bidirectional shifter. In steady state, the closed loop control will ensure an infinitesimally small error, and the output voltage will track the reference (V_{REF}).

Control System Based Model of Digital LDOs: To understand the loop and the overall system stability, we present a z-domain model for the digital LDO, as illustrated in Fig. 2b. The ADC acts as a voltage sampler and converts the continuous time error signal to its discrete time representation e*.

$$e^* = V_{REF}(nT) - V_{OUT}(nT) \tag{1}$$

The shifter acts as a discrete time integrator and in the simplest implementation α=1 [2]. The output of the shifter, which is a thermometer coded digital word (D(nT)) represents the number of pull-up PMOSes that are ON at the time instance, nT, where T is the period of the sampling ADC Clock. It can be written as:

$$\mathrm{D(nT)} = \alpha D\big((n-1)T\big) + K_{DIGITAL}\,e(nT) \tag{2}$$

This results in a transfer function:

$$\mathrm{D(z)}=\mathrm{K_{DIGITAL}}\frac{\mathrm{z}}{\mathrm{z}-\alpha}\mathrm{e(z)} \tag{3}$$

where, $\mathrm{K_{DIGITAL}}$ is the combined digital gain. The output of the shifter controls the number of PMOSes that are turned on, and thus interfaces with a continuous time plant (power MOSFETs and the load). This can be modeled as a zero-order hold (ZOH) cascaded with a single order plant whose output pole, a, is given by the load circuit. The ***s***-domain model for ZOH followed by the plant is:

$$\mathrm{P(s)}=\left(\frac{1-\mathrm{e}^{-\mathrm{sT}}}{\mathrm{s}}\right)\left(\frac{\mathrm{K_{DC}^{PLANT}}}{1+\frac{\mathrm{s}}{\mathrm{a}}}\right) \tag{4}$$

Thus, the open loop forward path transfer function of the LDO can be written in the z-domain as:

$$\mathrm{G(z)}=\mathrm{K_{DIGITAL}K_{DC}^{PLANT}}\left(1-\mathrm{e}^{-\frac{\mathrm{a}}{\mathrm{F_{sampling}}}}\right)\frac{\mathrm{z}}{(\mathrm{z}-\alpha)\left(\mathrm{z}-\mathrm{e}^{-\frac{\mathrm{a}}{\mathrm{F_{sampling}}}}\right)} \tag{5}$$

where $F_{SAMPLING}$ is the sampling frequency of the digital control. Using unity feedback, the overall closed loop transfer function of the digital LDO is:

$$\mathrm{H(z)}=\frac{\mathrm{G(z)}}{1+\mathrm{G(z)}} \tag{6}$$

Eqns. (5) and (6) provide insights into the stability of the digital LDO. Noting that for a digital system to be stable, the poles in the z-domain need to lie within the unit circle, we can perform a root-locus analysis of the system, which shows the closed loop poles as the open loop DC-gain (K_{DC}) of the system is varied. Fig. 3a shows the root locus of the digital LVR for two different output poles, 600MHz and 60MHz. The root-locus provides the maximum DC-gain that can be achieved without causing instability in the loop. It can be observed that a maximum DC gain of 10.71dB (30.46dB) can be achieved for an output pole position of 600MHz (60MHz). Ensuring stability in a digital control for digital load circuits is made difficult by the fact that the underlying circuit can go through wide dynamic ranges of operation, across V_{CC}, power states as well as fine-grained power gating. From data published in [8] on a wide dynamic range digital signal processor, we obtain the movement of the output pole (e^{-aT}) in the z-plane, and it has been plotted in Fig. 3b. For a constant gain and sampling frequency, one can note how the output pole position traces a locus on the z-plane leading to a stable system for higher load currents and a heavily under-damped (or unstable) system for light load conditions. Apart from the position of the continuous time load pole (a), and the loop gain K_{DC}, it is critical to choose an appropriate sampling frequency ($F_{SAMPLING}$) such that the discrete domain pole (e^{-aT}) maps to a desired location or region in the z-plane. High values of T (i.e., lower $F_{SAMPLING}$), leads to under-sampling of the pole position and can lead to loop instability. This leads to a multi-dimensional optimization across $F_{SAMPLING}$, K_{DC} and a to ensure both stability and desired time-domain response of the discrete system. It is also important to note, that a second order continuous time system is strictly always stable; however, a discrete implementation of a second order system is prone to instabilities. To perform an analysis on a hybrid control consisting of the digital LDOs and the continuous time PDN, we invoke 'Tustin' approximation on Eqn. (5) to obtain the continuous time equivalent of the open loop transfer function:

$$G(s)=K^{*}\frac{\left(1+\frac{sT}{2}\right)\left(1-\frac{sT}{2}\right)}{\left(1+\frac{sT}{2}\left(\frac{1+\alpha}{1-\alpha}\right)\right)\left(1+\frac{sT}{2}\left(\frac{1+e^{-\left(\frac{a}{F_{sampling}}\right)}}{1-e^{-\left(\frac{a}{F_{sampling}}\right)}}\right)\right)} \quad (7)$$

where,

$$K^{*}=\frac{K_{DIGITAL}K_{DC}^{PLANT}}{(1-\alpha)}$$

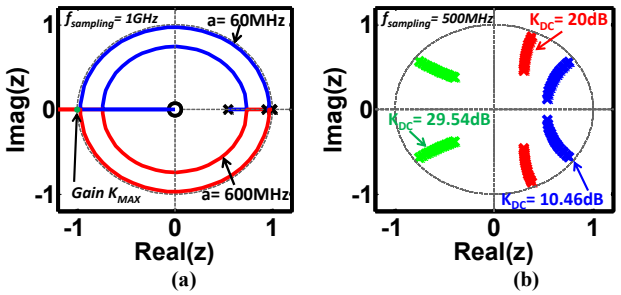


Fig. 3: (a) Root loci of the discrete time digital LDO on the Z-plane for different values of the sampling frequency and the output pole. (b) Loci of the output pole position in the Z-plane for different DC Gains.

The analysis of digital LDOs described above can potentially be done for each of the distributed regulators, but their interaction with the PDN leads to additional feedback loops and introduction of multiple poles and zeros from the PDN. Further, lower values of PSR (a typical characteristic of digital LDOs) lead to tighter coupling of LDOs with the PDN, resulting in (a) feedback loops through the PDN with higher loop gain and (b) stronger coupling between distributed LDOs on the same or different local grids.

III. CONTINUOUS TIME MODELS FOR THE PDN

In this section, we propose a generic framework to analyze the stability of a PDN composed of multiple digital LDOs. Two scenarios are considered in our framework:
(1) A single on-die grid with multiple digital LDOs driving it.
(2) Multiple local grids supplied by individual LDOs that share the same incoming line voltage.
The signal-flow paths of these LDOs can be traced via the global grid through bumps and package connections to the main PCB voltage regulator module (VRM). To understand the overall system stability across various closed loops formed in this complex system, we develop **s**-domain models for the PDN and include the distributed closed loop digital LDOs to understand stability margins for the whole system. This leads to a hybrid Multiple-Input-Multiple-Output (MIMO) system whose transfer functions from each input to output node needs to be evaluated and pole positions and pole-zero movements need to be ascertained. In the next subsections, we briefly describe the models for the various components of the PDN and how they have been incorporated in the system level analysis.

Distributed Model for the ON-die Grid: The on-die local grid is a complex network of distributed R and C as shown in Fig. 4. In scaled nodes, the decreasing size and pitch of metal wires increase wire resistivity as well as the metal-to-metal capacitance. Further, the insertion of multiple power-domains necessitates routing multiple supplies on a given area, thereby making the grid sparse and more resistive. Therefore, the distributed nature of the on-die RC grid needs to be captured for accurate modeling of interaction of multiple on-die digital regulators. Since different LDOs may drive different points of

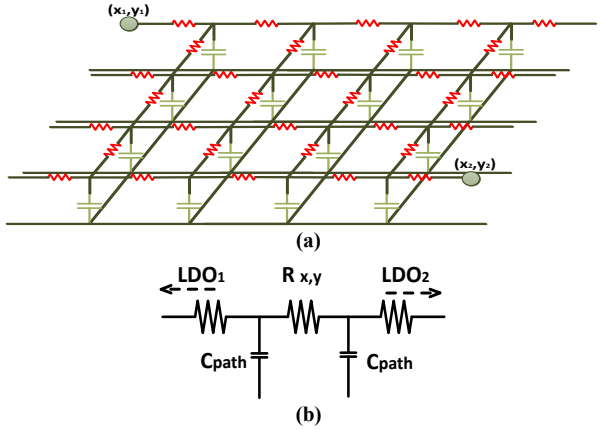
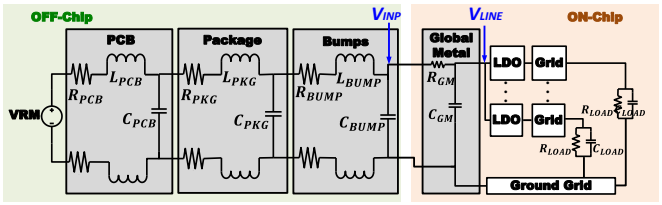


Fig 4: (a) Distributed nature of local grid with two sampling points (x_1,y_1) and (x_2,y_2) of connected LDOs (b) Simplified transfer function approximation model.



R_{PCB}	94μΩ	L_{BUMP}	0.5pH
R_{PKG}	10mΩ	C_{PCB}	240μF
R_{BUMP}	300μΩ	C_{PKG}	500nF
R_{GM}	10mΩ	C_{BUMP}	100nF
R_{LOAD}	10kΩ	C_{GM}	1pF
L_{PCB}	21pH	C_{LOAD}	0.1nF
L_{PKG}	120pH		

Fig 5: The PDN showing the on-chip and off-chip components and the integrated LDOs. The component values are shown in the table [9].

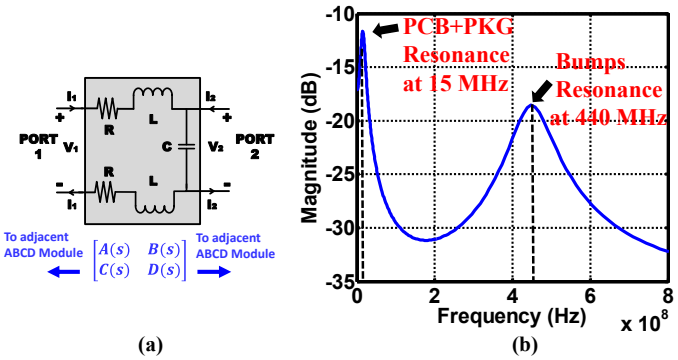
the same grid, the local grid adds additional phase between two regulator loops. Therefore, the effective R and C between these two distributed grid points, (x_1, y_1) and (x_2, y_2), needs to be modeled.

The effective resistance between any two points on a distributed grid can be approximated by [13]:

$$\frac{R_{x,y}}{r} = \frac{\sqrt{k}}{2\pi}\left(\ln(x^2 + ky^2) + 3.44388 - 0.0033425k - \frac{0.1975k(k-1)}{\pi}\right) \quad (8)$$

$R_{x,y}$ is the effective resistance between two points on a grid, $x = |x_1 - x_2|$, $y = |y_1 - y_2|$, $r_v = r$ and $r_h = kr$. Here r is the unit resistance, r_v and r_h give the vertical and horizontal resistances in the grid mesh and k is used to model the non-uniformity along the vertical and horizontal sections of the grid as described in [13]. The value of r has been obtained from the ITRS roadmap for the 22nm technology node.

The capacitance on the grid is contributed by the load and the decoupling capacitance (de-cap). For a 100um x 100um grid, a capacitance of roughly 100pF has been extracted. Using Elmore approximation, the total capacitance in the region of the two points under observation can be distributed across the effective resistance as shown in Fig. 4b. This model not only captures the distributed nature of the grid but also provides an s-domain transfer between two points on the grid that are driven by two LDOs under consideration.



(a) (b)

Fig 6: (a) The ABCD Model of each RLC section. (b) Bode plot of the off-chip components illustrating the resonant peaks.

ABCD Models of Off-Die Components: We model the PCB, package and bumps as a double-sided RLC ladder (for both V_{CC} and *GND*), as shown in Fig. 5. More complex off-die package models [10] can be easily incorporated into our design methodology. Upper metal layers are thicker and provide less resistance compared to intermediate and lower layers. Therefore, the global grid is modeled as a lumped RC ladder where the C_{GM} includes any additional de-cap that may be inserted at the global metal. The off-chip components are expressed in terms of their ABCD parameters that allow different off-chip sections to be easily cascaded to each other. A formal methodology to obtain ABCD parameters involves obtaining the Z-parameter model using the modified nodal analysis and then using the Z-parameters to obtain the ABCD parameters.

Two-port Z-model of off-die components can be obtained by evaluating port V/I relationship. This is calculated by performing modified nodal analysis (MNA) for a two port network. In MNA, R, L and C of the network are captured in matrices form. Each node gives a first order differential equation if the states are both the node voltages and the currents through inductors. The state-space formulation in s-domain turns out to be

$$G(s)x(s) + sH(s)x(s) = O(s)z(s) \quad (9)$$

$$y(s) = P(s)x(s) \quad (10)$$

Here, the input vector 'z' comprises of test current sources attached to the two ports. A unit magnitude is assumed for these sources for evaluating V/I relationship. State vector 'x' captures the voltages of all the nodes in the network and the currents through the inductors. The admittance matrix H comprises of both capacitor and inductor values and G is the conductance matrix for the network. O and P are the input and output mapping matrices. The model reduces to a two-port Z parameter matrix in the ***s***-domain by state space to transfer function transformation for the network as:

$$Z(s) = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \text{ where: } Z(s) = O^T(G + sC^{-1})O \quad (11)$$

O and P are set to capture only the port voltages; therefore, the computation complexity of evaluating the transfer function is low. The transmission parameter model (*ABCD* model) is then obtained from the Z parameters using Eqn. (12). ABCD model is suitable for cascaded stages as it simplifies the chain with simple multiplication of individual ABCD matrices.

$$\begin{aligned} &A = 1 + Z_1/Z_3, \quad B = Z_1 + Z_2 + (Z_1 * Z_2)/Z_3, \\ &C = 1/Z_3, \quad D = 1 + Z_2/Z_3 \\ &\text{Overall model: } \prod_i^n \begin{bmatrix} A & B \\ C & D \end{bmatrix}_i \quad i=PCB,PCK,BUMP \end{aligned} \quad (12)$$

Based on the *ABCD* model, the impedance plot of the entire off-chip network has been shown in Fig. 6b. It illustrates two resonant peaks, one at the bump frequency and another at the PCB and package frequency.

Coupling between LDO output and global power grid: Any noise generated on the local grid can be modeled as a small

signal variation picked up by the sampling node of the LDO (V_{OUT}). Such variations on the grid will couple with global power grid (called V_{LINE}). The resultant small signal transfer function is:

$$H_{VO}(V_{LINE}) = \frac{Z_{global} * (1 - A_{OL})}{Z_{global} * (K_{DC}^{PLANT} + 1) + r_o} \qquad (13)$$

Where A_{OL} is the open-loop gain of the LDO, Z_{global} is the impedance seen from V_{LINE} to the on-PCB VRM and r_o is the output resistance of the power MOSFETs in the LDO.

IV. SIGNAL FLOW GRAPH FOR THE SYSTEM

Based on the basic system illustrated in Fig. 7, we construct the Signal Flow Graph (SFG) of the entire PDN along with the digital LDOs, local grids, global GND grid and the multiple feedback paths through the PCB, PCK and BUMP (Fig. 7a,b). G represents the open loop transfer function of LDO and can be obtained from Eqn. (5). The PSR of the LDO (typically about -10dB for digital discrete time LDOs) captures the coupling from the V_{LINE} to the local grid. The load transfer function is modeled by a parallel R, C between the local grids and the global GND grid, which represents the load resistance and capacitance. Two feedback paths can be traced from the global GND grid to the V_{LINE}. First path originates from the capacitive coupling between global GND and global metal grid (Z_{GM}) and the second path traces through the off-die components (Z_{GND}+Z_{PCK}) as modeled in Section III. In this paper we will investigate two PDN topologies. *The first one* represents multiple LDOs driving a common local grid. A particular instance of this, where two LDOs are driving a single grid has been shown in Fig. 7a. It illustrates all the feedback connections in the PDN network, showing the individual LDO feedback loops and their interaction through the common line voltage (V_{LINE}), a common local on-die voltage grid (V_{01} and V_{02}) as well as through the external GND, package and PCB impedance (Z_{GND}+Z_{PCK}). *The second scenario* represents individual power grids separately driven by separate LDOs. The corresponding SFG is illustrated in Fig. 7b, where the different power domains interact through the common line (V_{LINE}) and the external off-die components. The SFG comprises of several key path and loop topologies that have been shown in Fig. 7c, and are used in implementation of Mason's Gain Formula in the distributed PDN, which will be described in Section V.

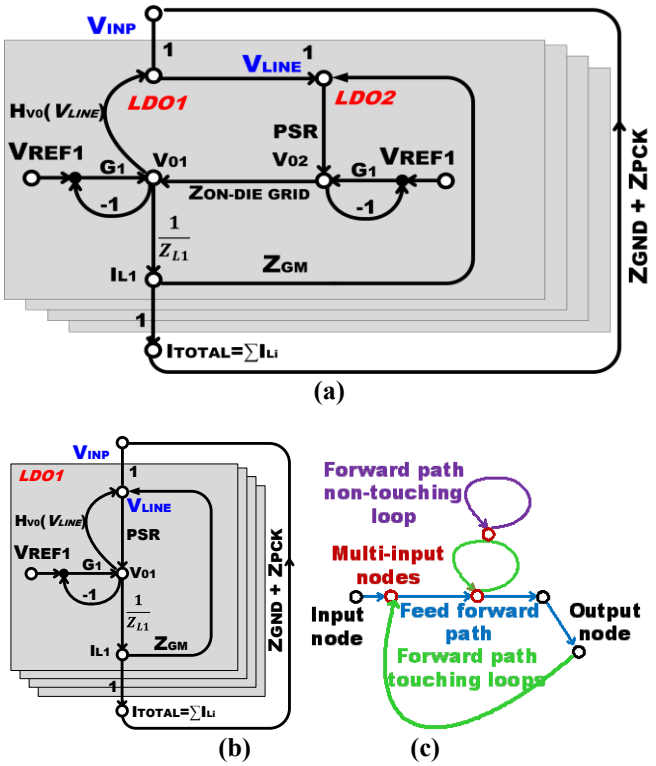


Fig 7: (a) Complete SFG of the system illustrating two LDOs driving a shared grid (b) Complete SFG of the system illustrating multiple LDOs driving separate grids (c) Different paths and loops for the application of Mason's Rule.

V. APPLICATION & AUTOMATION OF MASON'S RULE

We have, so far, presented a multi-LDO multi-grid PDN and multi-LDO single grid PDN in terms of signal flow representations. Appropriate optimizations are performed on the SFG to reduce the complexity of the underlying graph. Let us first consider the scenario of multiple-LDOs driving a common local voltage grid. LDOs are typically designed such that they remain stable across their entire region of operation but a stable feedback system may become unstable if it is inserted in a distributed network where multiple feedback loops are formed and they all add extra phase to the closed loops at unity gain. If multiple LDOs are placed in the PDN then evaluating the transfer function between the input and output nodes of each LDO will be required to evaluate if the overall system remains stable and if it still meets the design specifications. Therefore to gain insights into the overall system stability and the interaction of multiple LDOs among themselves and the PDN, we need to obtain the transfer function between two nodes on the SFG, Y_i and X_j. The transfer function between any two point Y_i and X_j on a SFG can be determined using Mason's Gain Formula [11]:

$$H_{ij}(s) = \frac{Y_i(s)}{X_j(s)} = \frac{\sum_k T_{k:j\to i}\Delta_{k:j\to i}}{\Delta_{ij}} \qquad (14)$$

where k = number of forward paths between nodes Y_i and X_j. Summation of k suggests that there can be multiple forward paths between any two nodes;

$T_{k:j\to i}$= forward traversal gain of path k;

Δ_{ij}= $1 - \sum(loop\ gains\ between\ Y_i\ and\ X_i) +$ $\sum$ $(nontouching\ loop\ gains\ between\ Y_j\ and\ X_i\ two\ at\ a$ time) -- $\sum$ $(nontouching\ loop\ gains\ between\ Yi\ and\ Xj$ three at a time) +…

$$\Delta_{k:j\to i} = \Delta_{ij} - \sum_l \Delta_l \,|\, (\Delta_l \cap T_k \neq 0 \,||\, \Delta_l \in \Delta)$$

or equivalently, $\Delta_{k:j\to i}$ is formed by eliminating from Δ_{ij} the loop gains that touch the kth forward path. A path with identical start and end node constitutes a loop. Conventions used for Mason's gain simplifications are shown in (Fig. 7c). Formal methods and algorithms on traversal of a SFG using Mason's Gain Formula have been discussed in [12]. Since our SGF is tailored to analyze the stability of the whole system tractably, we do not need to analyze the transfer function for every node pair. Since the LDO loops contain active elements, we need to analyze the transfer functions of the LDOs taking into account all the possible feedback paths including those contributed by the PDN. All feedback loops that originate and end on V_{ox} (output node of LDO_x) need to be analyzed. Therefore, in this context, the nodes under consideration have no non-touching loops. Table I summarizes the implementation flow of Mason's Rule in our proposed model. For the PDN with embedded and distributed LDOs, the SFG is first constructed. Next for every node of interest (i.e., the output nodes of the LDOs) all the input nodes are identified. For each input-output node pair, all the loops, non-touching loops and feed-forward paths are identified in terms of their transfer functions. Once all the different components for Eqn. (14) are identified, the transfer-function between the input-output node pair is determined using Eqn. (14). The process is repeated until all the relevant input-output pairs have been exhausted. At the end of the process, all the transfer functions that include active loop elements are determined and can be used to locate the system poles/zeros as well as gain and phase margins of all the LDO loops taking into account the PDN and other parasitic loops.

Table I. Pseudo code for application of Mason's Gain Formula for the entire PND network with embedded LDOs, corresponding to the SFG shown in Fig. 7.Some elemental paths and loops have been shown in Fig. 7c.

Construct directed SFG for N LDO system,
Define *Structure – node id, type (feed forward, loop, both), flags*
Construct adjacency linked list of directed SFG
While (! every node is traversed) Do
  Search for multi-input nodes (potential loop nodes)
  For each multi-input node
    Track loop by visiting adjacent nodes until starting node is reached
    Store loop nodes in a sub-linked list to the main list
  End For
End While
Pass Input (X_j=V_{refx}) and output (Y_i=V_{0x}) nodes
For each input-output node pair
Start from input node
Repeat until current node == output node
  If (adjacent node is already searched)
    Switch to other adjacent node with type 'feed forward' or 'both'
    Build feed forward gain for path *k*; $T_{k:j->i}$
End Repeat
For (each forward path k); Traverse nodes
  If (at least one common node found)
    Store id in loops touching forward path k
  else
    Store id in loops not touching forward path k
End for
Evaluate Δ_{ij}; no non-touching loop gains in presented PDN SFG
  $\Delta_{k:j\to i}$= Δ_{ij}-(loops touching forward path k)
Evaluate Eqn. (13) to obtain the TF between X_j & Y_i

VI. METHODOLOGY FOR STABILITY ANALYSIS OF A PDN WITH EMBEDDED LDOS

Even if discrete-time digital LDOs are designed to be stable for the local V_{CC} grid, it is not guaranteed that the overall system with the interacting LDOs and the PDN would remain so. Applying Mason's Gain Formula to the SFG enables us to ascertain the transfer function between any two pairs of nodes in the overall system. A transfer function between two pairs of nodes can either be:

(a) *Completely passive* – and hence inherently stable
(b) *Include Active gain elements* – and can lead to instabilities.

By simplifying the SFG and considering only the node pairs belonging to category (b), we obtain the pole locations for all the relevant node pairs. This essentially translates to determining the poles of the LDO considering their interaction with the system poles contributed by the PDN.

The exact location of the closed loop poles depend on the LDO poles (Eqn. 6), the LVR loop gain, $F_{SAMPLING}$, PSR and the impedance offered by the off-die components. Each LDO is designed to a given local specification. If a single LDO is placed in the PDN and the gain of PDN feedback loops are made negligible, by increased PSR for instance, then we obtain only the LDO closed loop poles. But in systems with low PSR and higher interaction between the LDO and the PDN, the phase contribution through the PDN loops cannot be ignored and need to be accurately modeled to evaluate the total phase margin of the system. Let us analyze the two scenarios: multiple-LDOs driving a single grid and multiple LDOs driving separate grids.

Multiple LDOs driving the same grid: Let us consider the scenario of multiple LVRs driving a single local grid, where

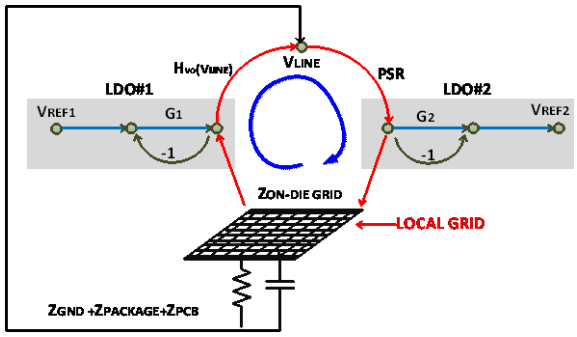


Fig 8: Two LDOs attached on the same grid. Path in red forms a n additional feedback loop to the output of LDO_1 and has been shown here.

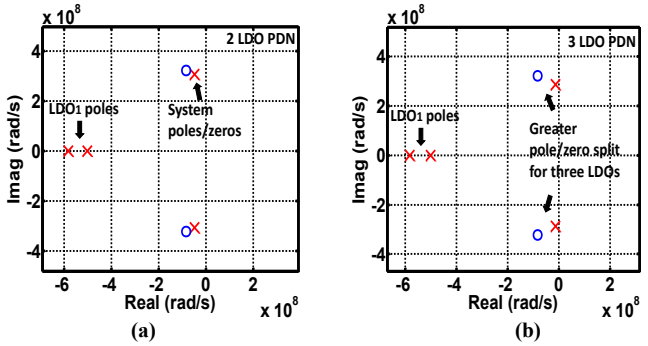


Fig 9: (a) Isolated closed loop (CL) LDO poles and system poles/zeros in a 2 LDO system on a single local grid with the PDN (b) CL poles of LDO under consideration when 3 LDOs are placed on a single local grid showing the decrease in phase margin of the LDO by pole zero split of the poles and zeros contributed by the system interaction.

two stable LDOs (say LDO_1 and LDO_2) are introduced in the PDN. The different feedback paths and interactions of the two LDOs have been illustrated in Fig. 8. We observe a pair of complex dominant poles in the system, as illustrated in Fig. 9a. These poles are introduced by the interaction between the LDO and the PDN. Any signal at the local grid couples to V_{LINE} through LDO_1 via the transfer function shown in Eqn. 12. This excites the dominant resonant frequencies of the off-grid RLC network. If in such topology the open-loop gain of the LDO_2 is low (and hence the resultant PSR of LDO_2 is also low) then the signal coupling back to LDO_1 is non-negligible. This decreases the phase margin of LDO_1 as it interacts with the PDN and distributed LDOs.

To evaluate the phase contribution and understand its origin qualitatively, let us analyze Fig. 9. The PDN contributes a pole and a zero, which cancel each other when the LDOs are non-interacting. As signal from LDO_1 couples to the line and feeds back through LDO_2, the PDN pole and zero split and the pole moves towards the RHP of the s-plane. As a result, the resultant phase contribution form the PDN feedback (i.e., phase contribution from the zero – phase contribution from the pole) is no longer zero but increases rapidly as the PSR of the LDOs decrease. It is intuitive to understand that as the number of LDOs on a shared grid increases, the overall phase margin decreases. This is shown in Fig. 9, where the case of three LDOs driving a common voltage grid creates further splitting of the zero and the pole giving rise to higher instability. As the pole moves towards the imaginary axis, the overall system can rapidly become unstable.

This can also be seen in the phase contribution of the PDN poles/zeros at unity gain-bandwidth. In other words, the additional feedback loop as shown in Fig. 8, can add higher phase shift at unity gain, creating loss of phase margin. Let us consider two LDOs on a shared local grid with unity gain bandwidth (ω_c) of 500MHz. As the two LDOs interact through the common grid and the PDN, in a manner shown in Fig. 8, additional phase is contributed by the PDN, which results in compromised phase margin at unity gain. As shown in Fig. 10, an additional 5 to 6 degrees of phase contribution can be expected when the LDOs have a PSR of ~10dB (which is common for digital LDOs). When three LDOs are placed in the common grid, the phase contribution from two additional loops, that are created, can be as high as 15 degrees. Any additional phase, thus added to the LDO loops at unity gain, results in a direct reduction of the phase margin and increase in potential instability of the system.

This interaction between LDOs is expected to be minimal if they operate in high gain regimes. This can be observed from Fig. 11a, where the pole movement is negligible and therefore, the phase margins of the LDO have not degraded. Higher loop gain also increases the PSR of the LDOs, and a higher value of PSR reduces the gain of the feedback loop through the PDN. Since lower PSR is a typical characteristic of digital LDOs, we note that the system pole moves considerably towards the imaginary axis for low PSR. It can be seen in Fig. 11b, that as the PSR varies from 30dB to 10dB in a 3LDO system, the system pole moves towards the imaginary axis and can lead to system instability.

The role of the impedance of the off-die components is also critical and our methodology can be used to evaluate that. Increasing the impedance offered by off-die RLC grid from its nominal value (Z_{nom}) increases the interaction of the LDO output with the PDN. As the overall V_{LINE} impedance increases, the transfer function given in (12) increases the noise coupling from the grid to V_{LINE} taking the system towards potential instability as shown in Fig. 12.

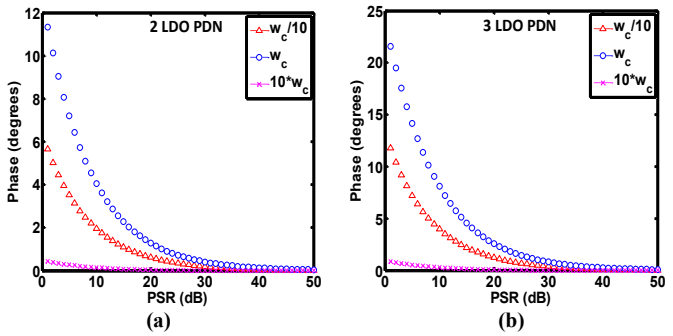


Fig 10: (a) Additional phase added to the LDO#1 in a 2 LDO system loop at ω_c, $10*\omega_c$, $\omega_c/10$ for varing PSR where ω_c=500MHz is the unity gain bandwidth. (b) Additional phase added to the LDO#1 in a 3 LDO system loop at ω_c, $10*\omega_c$, $\omega_c/10$ for varing PSR where ω_c=500MHz is the unity gain bandwidth.

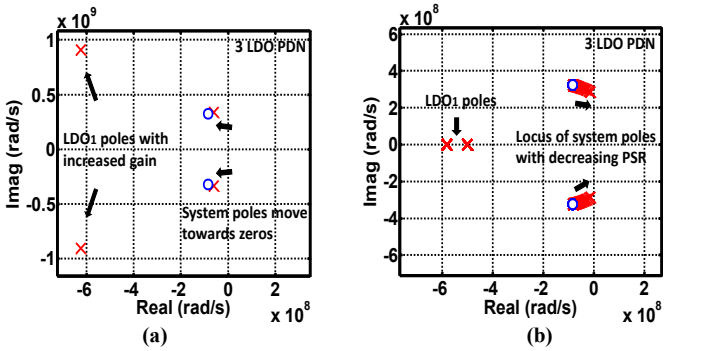


Fig 11: (a) Increased gain of the LDO#1 reduces the phase margin degradation contributed by the system feedback loop (b) Movement of phase degradation poles (system poles) as a function of increasing PSR in a 3 LDO, single grid PDN show an improvement of phase margin of the LDO under consideration.

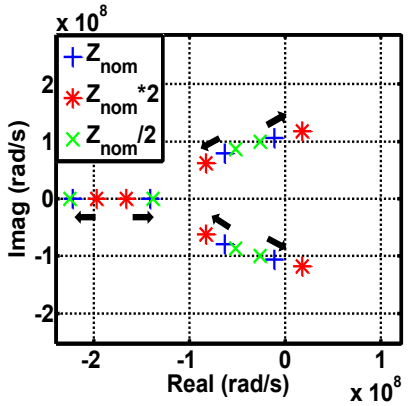


Fig 12: System poles as a function of the impedance (Z) of the off-chip components. Arrows indicate the direction of pole movement as Z increases.

Individual LDOs driving separate local grids: In this section we investigate the stability for multiple LDOs driving separate local grids. They share the same incoming voltage line (V_{LINE}). The SFG is shown in Fig. 7b.

Since the grids are separate in this case, the only system feedback loop that can be traced goes through the global GND grid and the package. Attenuation provided by this feedback path is high and does not contribute significantly to the degradation of phase margin at unity gain. Fig. 13 illustrates the bode plot of the feedback loop and shows very high attenuation through the parasitic path. This is significant considering that the primary feedback of the LDO loops offer 20-30dB of gain. Thus the parasitic path in the distributed LDO PDN do not have enough gain to be consequential and does not degrade the phase margins of any of the embedded LDOs. Although separate LDOs drive separate grids and share a common line, they do not seem to interact with each other strongly enough to cause instability. Nevertheless, we present it here for the sake of completeness and show that the proposed methodology can be used to evaluate such complex PDNs and embedded LDOs.

VII. CONCLUSIONS

This paper presents a comprehensive methodology for analyzing the overall stability of distributed digital LDOs in a power delivery network. Hybrid control models of all the necessary components have been developed and an automated method of analyzing system poles using Mason's Gain Formula has been proposed. We have demonstrated that when multiple LDOs drive a common voltage grid, significant loss of phase margin can occur. Analysis on various design corners reveals the design trade-offs and provides a systematic methodology to comprehend stability in a muti-grid PDN. This methodology can be employed in pre-silicon validation to understand the limits of system stability under wide dynamic range and to ensure that even under the worst case load conditions the overall system meets the target phase margin and stability. It can also be used to adjust LDO design parameters such that the overall system stability is ensured.

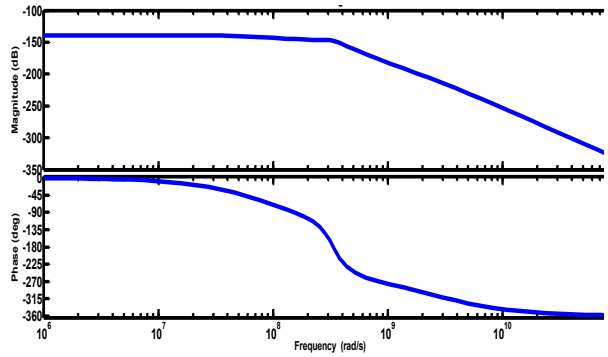


Fig 13: Bode plot of parasitic feedback paths in a multi-grid PDN where each grid is driven by a separate LDO and they interact only through the GND grid and the external package components.

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