

## 5.6 A 0.13 $\mu$ m Fully Digital Low-Dropout Regulator with Adaptive Control and Reduced Dynamic Stability for Ultra-Wide Dynamic Range

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An increasing number of power domains and of power states per domain, as well as decreasing decoupling capacitance per local grid and ultra-wide current dynamic range of digital load circuits (for low power on one end while maintaining performance at another) necessitate the design of high-efficiency, compact on-die voltage regulators providing ultra-fine grained spatio-temporal voltage distribution [1,2]. Digitally implementable linear regulators operated in low-dropout (LDO) mode, based on continuous time or discrete time control, exhibit process and voltage scalability [3-5], thus supplementing their analog counterparts [6].

This paper presents a discrete-time, fully digital, scan-programmable LDO macro in 0.13 $\mu$ m technology featuring greater than 90% current efficiency across a 50 $\times$  current range, and 8 $\times$  improvement in transient response time in response to large load steps. The baseline design (Fig. 5.6.1) features a 128b barrel shifter that digitally controls 128 identical power PMOS devices to provide load and line regulation at the node  $V_{REG}$ , for a scan-programmable fine-grained synthetic load. A clocked comparator, which eliminates the need for any bias current, controls the direction of shift, D. The programmable mux-select signals, MUX1 and MUX2, provide controllable closed loop gains,  $K_{BARREL}$ , of 1 to 3 $\times$ . Since at any clock edge only 1, 2 or 3 shifts can occur (depending on the gain setting), fine-grained clock gating is enabled by dividing the 128b shifter into four sections and only enabling the clock to the section(s) where the shift occurs (Fig. 5.6.1).

A linearized hybrid control model of the LDO (Fig. 5.6.2) reveals two open loop poles: 1) An integrator pole at  $z=1$ , and 2) At  $z=e^{F_{LOAD}/F_S}$  where  $F_{LOAD}$  is the equivalent output pole ( $F_{LOAD} = 1/(R_{LOAD}||R_{PULL\_UP})C_{LOAD}$ ) and  $F_S$  is the sampling frequency of the discrete time controller. With ultra-wide dynamic ranges of the load current,  $R_{LOAD}$  changes, often over two orders of magnitude; hence the open loop poles (and equivalent closed loop poles) of the regulator span a large range (Fig. 5.6.2). Consequently at iso- $F_S$ , heavy load conditions show an over-damped response, whereas light load conditions become under-damped and even oscillatory. To cater to a wide load range, we provide adaptive control such that  $F_{LOAD}/F_S$  is bounded. This results in a more consistent transient response and, by scaling  $F_S$  with  $F_{LOAD}$  (and hence  $I_{LOAD}$ ), the current efficiency of the LDO is vastly improved. In the present design, a slower control loop checks for the status of bit-45 and bit-85 of the barrel shifter. Bit-45=1 and bit-85=1 indicates that both PMOS devices are off and hence light load conditions exist. Similarly, 01 and 00 on bit-45 and bit-85, respectively, represent nominal and heavy load conditions. Once the quiescent (Q) point of the load changes and a heavy, nominal or light load condition is identified, an adaptive controller waits for an incubation period (which eliminates chattering between multiple frequency-modes) and sets  $F_S$  to  $F_{HIGH}$ ,  $F_{NOM}$  or  $F_{LOW}$ . The incubation period is programmable and is realized using an externally clocked binary counter, enabling  $F_S$  adjustment only when the counter saturates. When operating in regulation, with small load transients, the autonomous choice of  $F_S$  results in decreased ringing, faster settling and close tracking of the controller current,  $I_{CTL}$ , with  $I_{LOAD}$ .

Along with adaptive control for efficient regulation across a wide dynamic range, we propose a programmable and digitally implementable 'variable structure control' that facilitates fast recovery from large voltage droops, in response to large load steps. These are infrequent, often triggered by changes in the power state of the system. This design principle, referred to as Reduced Dynamic Stability (RDS) and borrowed from the control design of military aircrafts, exhibits an ultra-fast transient response without compromising static stability. This is accomplished by retrofitting the baseline design with overshoot and droop detectors that compare  $V_{REG}$  with  $V_{REF}\pm\Delta$  (Fig. 5.6.3). Once such a droop/overshoot is detected, the regulator selects a fast clock ( $F_{TRANSIENT}=400\text{MHz}$ ), which will instantaneously render the loop marginally stable by moving the open (and hence closed) loop poles very close to  $|z|=1$ . Further, the barrel shifter gain can be simultaneously increased to further reduce the stability margin of the loop. This enables a faster recovery from load transients. As soon as  $V_{REG}$  returns close to regulation ( $V_{REF}+\Delta > V_{REG} > V_{REF}-\Delta$ ),

the RDS logic switches back to the sampling clock  $F_S$ , allowing a stable return to regulation without any ringing. The current design supports externally programmable  $\Delta$  and measurements support a provably stable response for  $\Delta = 50$  or 100mV.

The LDO macro is measured across a wide range of operating conditions and the Shmoo plot (Fig 5.6.4) illustrates  $V_{REG}$  of 0.45 to 1.15V with the line voltage,  $V_{IN}$ , from 0.5 to 1.2V, thus revealing (a) a minimum dropout of 50mV and (b) near threshold operation (process  $V_T \approx 300\text{mV}$ ). Oscilloscope capture of a representative measurement (Fig. 5.6.4) shows: 1) Regulation under Q-point changes; 2) Ripple of less than 3%, and 3) Autonomous adaptation of  $F_S$  in response to load changes. Scope captures also show baseline design (RDS off) vs. proposed design (RDS on) and reveal decreased settling time ( $T_S$ ) and  $V_{DROOP}$  when RDS is enabled.

The settling time for small current transients (Fig. 5.6.5) reveals a strong dependence of  $F_S$  on  $I_{LOAD}$  (and hence  $F_{LOAD}$ ), further motivating the use of dynamically adaptive  $F_S$  under different load conditions to meet a  $T_S$  specification. A color-map provides the autonomous and dynamic allocation of  $F_{HIGH}$ ,  $F_{NOM}$  and  $F_{LOW}$  for varying  $F_{LOAD}$  (i.e.,  $I_{LOAD}$  and  $V_{LOAD}$ ) to meet a target  $T_S$ . Measurements are carried out on the baseline and proposed design (with RDS) for voltage droops  $>100\text{mV}$ . The baseline design, with  $I_{LOAD} = 0.7\text{mA}$  and  $\Delta I_{LOAD}=1.2\text{mA}$ , shows an initial decrease in  $T_S$  with  $F_S$  as the system becomes critically damped, and an eventual increase in  $T_S$  with  $F_S$  as the system becomes under-damped and exhibits ringing and slower settling. The proposed design with RDS enabled (for  $K_{BARREL}=1$  and 3) shows 8 $\times$  improvement in  $T_S$ . Faster response also reduces  $V_{DROOP}$  in response to the same load step and 36% (60%) reduction of  $V_{DROOP}$  is observed for  $\Delta I_{LOAD}$  of 2.1mA (0.7mA). Load regulation for a range of  $V_{REG}$  voltages shows an average of 6mV/mA and a worst case of 10mV/mA. We also note a 50 $\times$  load range, which can be further scaled if a larger barrel-shifter and power MOSFETs are used. By enabling fine-grained clock gating, 34% reduction of controller power,  $P_{CTL}$ , is measured. As adaptation to Q-point, due to dc changes in  $I_{LOAD}$ , is enabled for the wide load current range, we note  $F_S$  adjusting for high, nominal and light loads, thereby providing high current efficiency across the entire load range while meeting a target  $T_S$  specification. A 4 $\times$  improvement in current efficiency is measured at light load conditions when compared to the baseline design (Fig. 5.6.6). A comparative study with recently published data establishes that the current design (Fig. 5.6.7) is competitive in both power efficiency and performance. Adaptive control enables an energy-efficient wide dynamic range. A power efficiency figure of merit (FOM1), defined as the average current efficiency across a load range from  $I_{MAX}$  to  $0.2I_{MAX}$ , is  $>90\%$ , compared to  $<56\%$  for previously published data. RDS, which enables a dynamic trade-off between instantaneous stability and transient response, provides ultra-fast  $T_S$  with a discrete time digital loop without compromising the runtime stability. FOM2 [2], normalized to the process node, shows that the performance is comparable to its analog counterpart [6].

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### References:

- [1] Z. Toprak-Deniz, et al., "Distributed system of digitally controlled microregulators enabling per-core DVFS for the POWER8 TM microprocessor," *ISSCC Dig. Tech. Papers*, pp. 98-99, Feb. 2014.
- [2] P. Hazucha, et al., "High Voltage Tolerant Linear Regulator With Fast Digital Control for Biasing of Integrated DC-DC Converters," *IEEE J. Solid-State Circuits*, vol.42, no.1, pp. 66-73, Jan. 2007.
- [3] S. Gangopadhyay, et al., "Modeling and analysis of digital linear dropout regulators with adaptive control for high efficiency under wide dynamic range digital loads," *Design, Automation and Test in Europe*, pp. 1-6, Mar. 2014.
- [4] C.-C. Chiu, et al., "A 0.6 V resistance-locked loop embedded digital low dropout regulator in 40nm CMOS with 77% power supply rejection improvement," *IEEE Symp. VLSI Circuits*, pp. 166-167, June 2013.
- [5] Y. Okuma, et al., "0.5-V input digital LDO with 98.7% current efficiency and 2.7- $\mu$ A quiescent current in 65 nm CMOS," *IEEE Custom Integrated Circuits Conf.*, pp. 1-4, Sept. 2010.
- [6] J. F. Bulzacchelli, et al., "Dual-Loop System of Distributed Microregulators with High DC Accuracy, Load Response Time Below 500 ps, and 85-mV Dropout Voltage," *IEEE J. Solid-State Circuits*, vol. 47, no. 4, pp. 863-874, Apr. 2012.

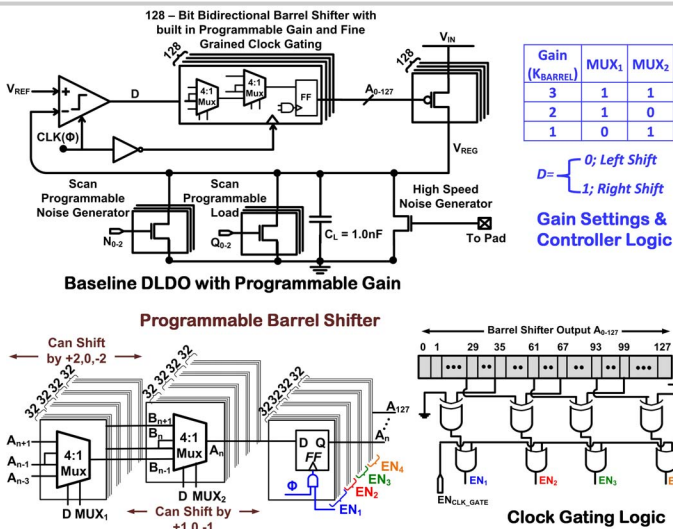


Figure 5.6.1: Fully digital low-dropout regulator with digitally programmable loop gain and fine-grained clock gating.

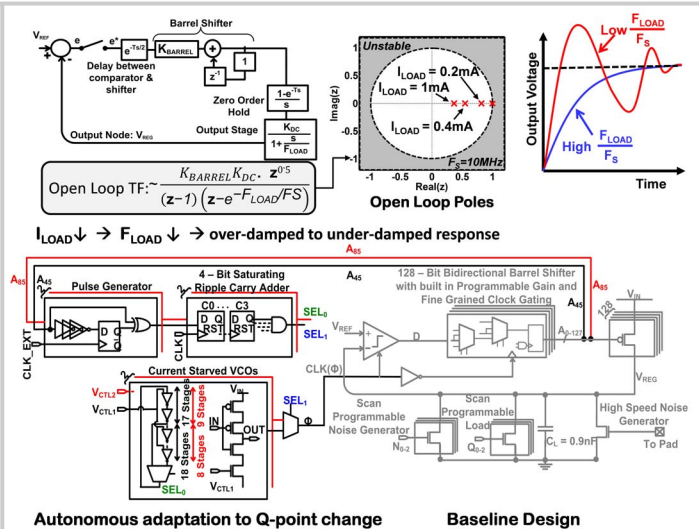


Figure 5.6.2: Autonomous adaptation of sampling frequency ( $F_s$ ) across a wide dynamic range.

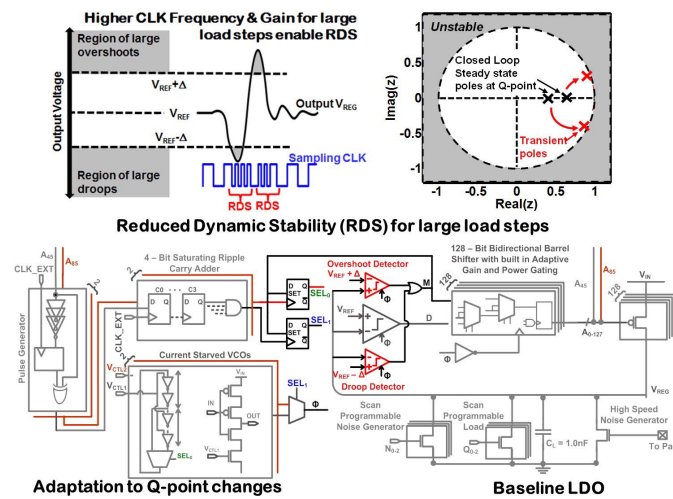


Figure 5.6.3: Droop and overshoot detectors detect large load transients. In response, a faster sampling clock and higher loop gain are enabled for faster recovery from droops and overshoots.

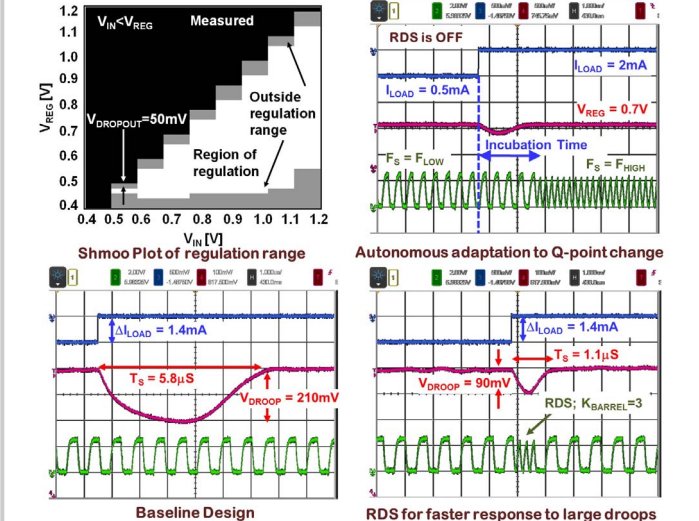


Figure 5.6.4: Measured operating range of the LDO with representative scope captures.

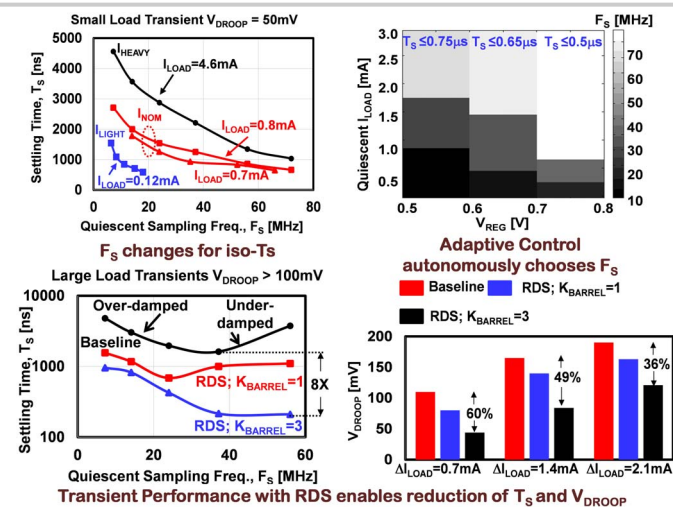


Figure 5.6.5: Measured settling time,  $T_s$ , for small droops with adaptation for autonomous choice of  $F_s$ . RDS allows 8x improvement in  $T_s$  for large load transients and 36% to 60% reduction in  $V_{DROOP}$ .

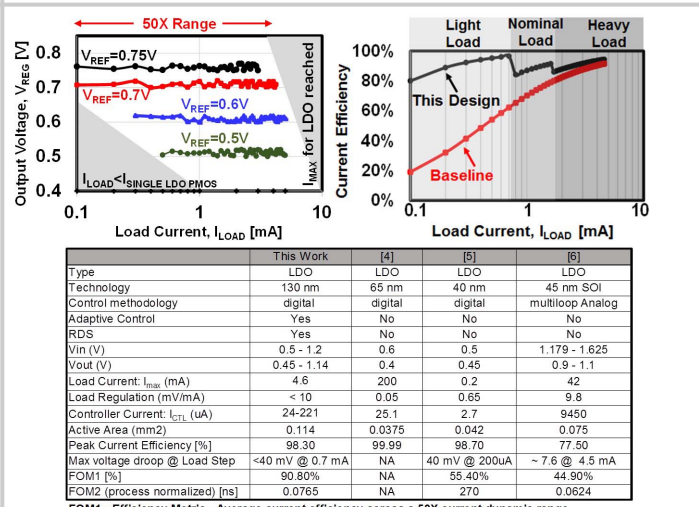
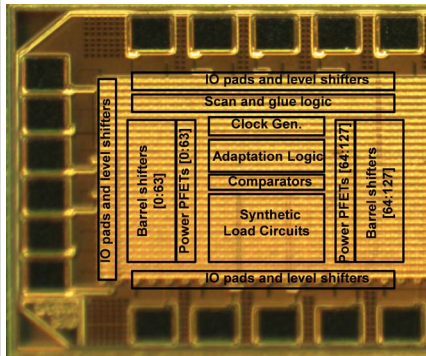


Figure 5.6.6: Measured load regulation, current efficiency and performance summary.



Process	IBM 130nm CMOS 8-M
Total Area	2 mm <sup>2</sup>
Active Area	0.3552 mm <sup>2</sup>
LDO Area	0.114 mm <sup>2</sup>
Testing Interface	QFN Package

Figure 5.6.7: Chip micrograph, process and design specifications.