On Limit Cycle Oscillations in Discrete-Time Digital Linear Regulators

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***Abstract*—Increasing level of transistor integration with multiple voltage domains and power states, ever decreasing decoupling capacitance, fast load transients and the need for fine-grained spatio-temporal power management provide impetus for embedding distributed point of load (PoL) linear regulators deep within digital functional blocks of microprocessors and Systems-on-Chip (SoCs). This demands modularity in design as well as process and voltage scalability of such linear regulators. Digital linear regulators have emerged as an attractive counterpart to the traditional analog solutions. This paper presents the circuit implementation and a steady state response model of a discrete-time digital regulator with simulations and hardware measurements with an emphasis on the steady state oscillations. We develop parametric models to demonstrate design trade-offs for a stable steady state response.**

I. Introduction

Recent advances in process technologies enable the transistors in microprocessors and SoCs to reach unprecedented levels of integration. Power demands of such systems undergo large dynamic ranges. Further decreasing circuit footprints lower decoupling capacitances; and demand higher transient and leakage currents. Fine grained voltage levels allow an increased number of chip and system power states. Therefore, the need for fine-grained spatio-temporal power management for digital loads in this complex power delivery network is met in a hierarchical manner [1], [2] where high power efficiency switched mode power supplies (SMPS) [3] or switched capacitor DC-DC converters [4] provide low operating voltages inside the package from bulky off-chip voltage regulation module (VRM) and are followed by fast but less efficient linear regulators often operated in a low dropout (LDO) mode right at the point of load (PoL).

These regulators are traditionally analog in nature and are optimized for particular load specifications [5], [6] but with the introduction of digital LDOs (DLDO) [7], [8], [9], [10], [11] wider dynamic range linear regulators can be built with minimum overhead in a digital design process. Power mosfet in these designs is discretized into an array operated in triode region for very low drop-outs. Their design scalability and potential synthesizability allow ultra-fine grained spatio-temporal voltage regulation at the PoL. Broadly, digital LDOs can be divided into continuous and discrete time versions. In discrete-time digital LDOs, a 'master clock' synchronizes the control part of the regulator [7], [10], [11] whereas in continuous time regulators, a continuous time measure, like phase or frequency is used to control the power devices [9], [12]. Although digital LDOs show acceptable transient performance and a wide design parameter space, but in steady state the regulated output suffers from limit cycle oscillations [7]. In this paper, we present a nonlinear sampled feedback control model to comprehend the steady state dynamics of a discrete time digital LDO. The bounds on different modes of limit cycle oscillations under different design parameter constraints are calculated. We propose a dead-zone controller to mitigate these limit cycles and illustrate the parametric design space. The circuit is simulated in a commercial IBM 130nm process design kit (PDK) using HSPICE and experimental verification is completed through a prototype regulator built on a printed circuit board (PCB) with discrete components.

Section I represents the design of the DLDO in simulation and on the experimental PCB. Section II proposes and elaborates the steady state model to capture inherent limit cycle dynamics verfied through simulation as well as experiments. It also explores the parametric design space for stability and performance. Finally, a variant of the baseline design is presented in section III to mitigate limit cycles followed by conclusion in section IV. All the major sections contain both simulation and hardware measurement results.

II. Design of a Discrete Time Digital LDO

The proposed digital LDO consists of an analog to digital conversion stage which is a single bit comparator in its simplest implementation. It is followed by a programmable gain

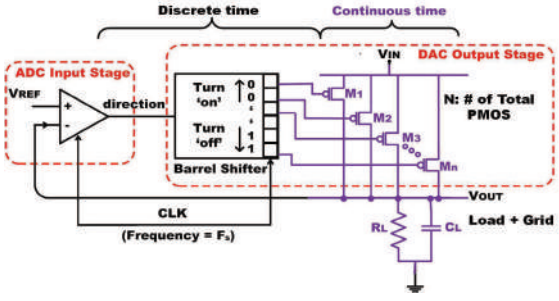

Figure 1. Proposed discrete time digital LDO with embedded A/D converter, barrel shifter and a PMOS array.

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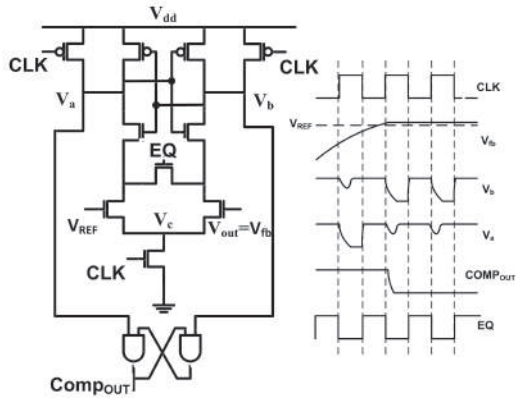


Figure 2. Sense amplifier based comparator used as a single bit A/D converter for the proposed LDO.

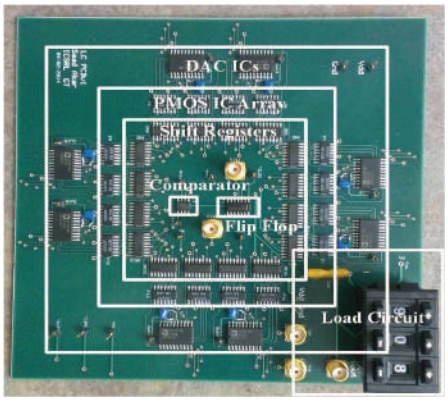
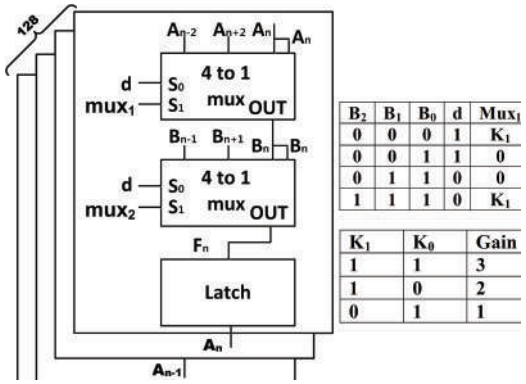


Figure 4. Prototype DLDO

barrel-shifter which is a variable gain 128-bit shift register with each output bit connected to a power MOSFET. As opposed to a single power MOSFET in analog LDOs, the output power stage is discretized into smaller power MOSFETs (PMOS) as shown in Fig. 1. In its current implementation, the comparison of output regulated voltage (V_{OUT}) against a reference is synchronously obtained through a sense-amplifier based clocked comparator shown in Fig. 2. This clocked comparator improves power efficiency of the system by obviating the need for a constant bias current in a clock-less version. During the negative phase of the clock, nodes V_a and V_b are charged to Vdd. A discharge race occurs during the positive clock phase and depending on the voltage difference between the two inputs, a decision is latched in a set-reset (SR) latch. The final output is a single-bit bi-directional signal which increments or decrements the barrel shifter output. A programmable range of +3 to -3 shifts is realized through a barrel shifter using two levels of mux presented in Fig. 3. If $V_{OUT} < V_{REF}$, a certain number of PMOS devices (N_P) are turned on and if $V_{OUT} > V_{REF}$ a certain number of PMOS devices (N_P) are turned off. N_P is obtained from the register-programmable variable gain of the barrel shifter and provides the forward gain of the system (K_{barrel} shifter). In the presented LDO, a variable gain ranging from +3 to -3 (sign represents the direction) is developed in a 128 bit barrel shifter which actuates a total of 51.2 µm PMOS array capable of delivering a maximum of 3.5 mA at a nominal output voltage of 0.7 V from a supply voltage of 1 V. The complete circuit is developed and simulated using IBM 130nm process design kit (PDK).



B_2	B_1	B_0	d	Mux_1
0	0	0	1	K_1
0	0	1	1	0
0	1	1	0	0
1	1	1	0	K_1

K_1	K_0	Gain
1	1	3
1	0	2
0	1	1

Figure 3. Design schematic of a 128 bit barrel shifter using 4x1 muxes and latches to provide programmable magnitude and direction of shift. Magnitude of gain is register programmable and the direction is determined by the ADC output.

A. Experimental Setup

An experimental setup using discrete ICs on a printed circuit board (PCB) is developed to validate the digital LDO design, shown in Fig. 4. An analog comparator followed by a flip flop acts as a synchronous comparator to realize the ADC stage. A cascade of 8-bit shift registers forms a 64-bit barrel shifter capable of providing a gain of 1 PMOS/cycle. Finally, an array of digital to analog converters (DAC) takes input from gates of the PMOS array. DAC output is a measure of the number of 'on', 'off' and 'switching' PMOS devices in the array. A programmable potentiometer with a fixed capacitance serves as a variable RC load. Achieved regulation and response to an instantaneous load transient is shown in Fig. 5 and 6 for HSPICE simulation and experimental setup respectively.

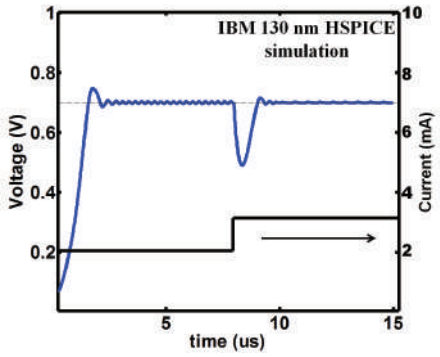


Figure 5. Regulation in response to a 1mA load step.

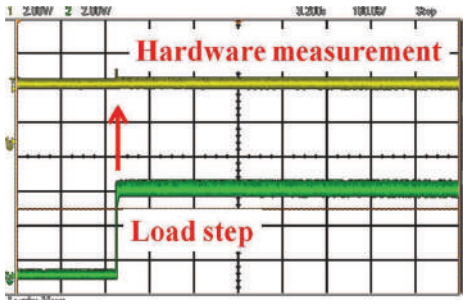


Figure 6. Measured load step and regulation on the DLDO PCB.

III. STEADY STATE NONLINEAR SAMPLED FEEDBACK CONTROL MODEL

Increasing the sampling clock frequency (F_s) improves the transient performance of the LDO as shown by the decrease in rise time (T_r) illustrated in Fig. 7; but it has been shown to cause instability in the overall system dynamics if $F_s$is too high[10]. Therefore, the role of F_s has to be qualitatively and quantitatively understood to ensure a reliable and stable steady state response. Due to the inherent on-off control mechanism of a digital LDO, a number of PMOS devices, called mode hereafter, switch periodically in the steady state and give rise to limit cycles at the output. Fig. 8, confirms this oscillatory behavior of V_{OUT} through simulation results. Changing sampling or the load frequency changes the mode of oscillation in the steady state. This behaviour is verfied through experiments where a change in mode is observed using an array of DACs on the experimental PCB shown in Fig. 9. A linearized model at the operating point is insufficient in capturing these oscillations; therefore, to accurately quantify the possible modes of limit cycle oscillations, a steady state nonlinear sampled feedback model is developed, as shown in Fig. 10. The comparator exhibits the characteristics of an ideal relay with zero dead-time if any offset is neglected. It is followed by an impulse sampler running at F_s modeling the ADC stage. Synchronous triggering of the following barrel shifter adds a clock cycle delay in the forward path. Since

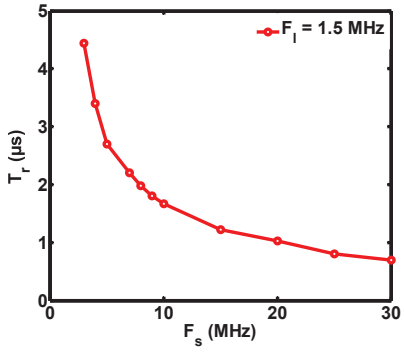
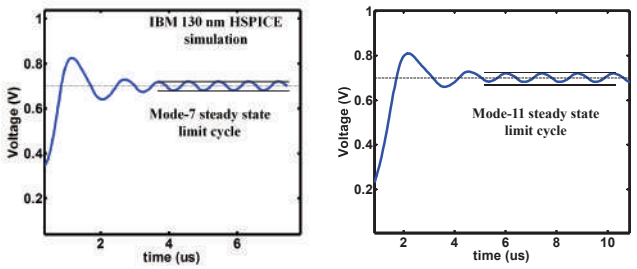


Figure 7. Increased transient rise time (0 to 700mV step) performance with increasing Fs.



(a) (b)

Figure 8. Steady state ripple shows the existence of (a) mode-7 and (b) mode-11 limit cycle oscillations.

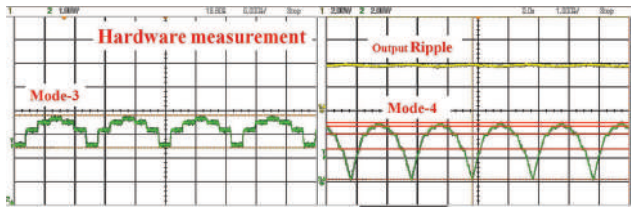
the barrel shifter accumulated the voltage error over clock cycles, it acts like an ideal integrator. As the number of 'on' PMOS remains constant during the inter-sample period, the conversion of digital samples to continuous-time is modeled by a zero order hold (ZOH). Finally, this number goes through a control to output transfer function, thus converting the digital output of the barrel shifter to a resultant current through the PMOS array (current of each PMOS device = I_{PMOS}). This current actuates the load circuit. The plant is modeled as a first order low pass filter of the output RC load with a pole at frequency F_l.

A. Model Development

A limit cycle induces a repetitive pattern at the output of the relay which gives a specific V_{OUT} ripple frequency for each mode. The bounds on a given mode 'n' in terms of F_s/F_l is obtained by applying the Nyquist criterion on the feedback system evaluated at an induced ripple frequency of $w_s/2n$. Then for 'n' number of PMOS to switch in steady state, a mode-n oscillation is obtained if (1) is satisfied.

$$N(A,\phi)L(jw_s/2n) = -1 \tag{1}$$

Here $N(A,\phi)$ represent the transfer characteristics of hard relay non-linearity and $L(jw_s/2n)$ represents rest of the linear components in both the feed forward and feedback portions. Describing function (DF) analysis is used to linearize the non-linear relay [13]. Application of DF analysis requires a single monotone as input to the relay. In our case, this is validated



(a) (b)

Figure 9. Measured output of DACs showing the existence of (a) mode-3 and (b) mode-4 oscillations. F_s/F_l < 3 for both the measured scenarios.

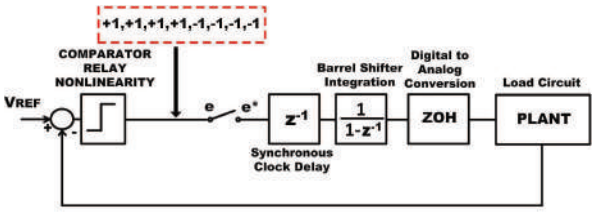


Figure 10. Steady state model of the proposed LDO with ideal relay, a delay, an integrator and a sample and hold (ZOH) followed by the load plant.

by the low pass filtering effect of the plant with F_s atleast 5-10X times higher than F_l. $N(A,\phi)$ is obtained at a particular frequency given by the following expression

$$N(A,\phi) = \frac{phasor(relay_{OUTPUT})}{phasor(relay_{INPUT})} = \frac{|Y^{'}(t)|}{x(t)} \tag{2}$$

For mode-n to exist, the comparator makes a total of 2n decisions on n PMOS running at F_s. This is equivalent to an input sinusoid of frequency $\frac{\omega_s}{2n}$ to the relay given as

$$x(t) = Asin(\frac{\omega_s}{2n}t + \phi); 0 < \phi < \frac{180^o}{n} \tag{3}$$

All the switching PMOS atleast switch once in 180^o. Since output of the relay is in terms of discrete samples, the fundamental component of it is advanced in phase by $(180/2n)^o$.

$$|Y^{'}(t)| = \frac{2}{nT}\int_{0^-}^{nT^-} y^{'}(t)sin(\frac{\omega_s}{2n}t + \frac{180^o}{2n})dt \tag{4}$$

This integration is solved by a direct summation of the samples evaluated at timeT_s and $\omega_s = {}^{2\pi}/_{T_s}$; For samples of amplitude M, this simplifies to

$$|Y^{'}(t)| = \frac{2M}{nT}\sum_{0^-}^{n^-} sin(\frac{2\pi}{2n} + \frac{180^o}{2n}) \tag{5}$$

Evaluating (2) using (3) and (5) gives

$$N(A,\phi) = \frac{\frac{2M}{nT}\sum_{0^-}^{n^-} sin(\frac{2\pi}{2n} + \frac{180^o}{2n})}{Asin(\frac{\omega_s}{2n}t + \phi)} \tag{6}$$

As an example, mode-2 evaluates to $N(A,\phi) = \frac{\sqrt{2}M}{TA}\angle(45^o - \phi); 0 < \phi < 90^o$ and mode-3 gives $N(A,\phi) = \frac{4M}{3TA}\angle(30^o - \phi); 0 < \phi < 60^o$

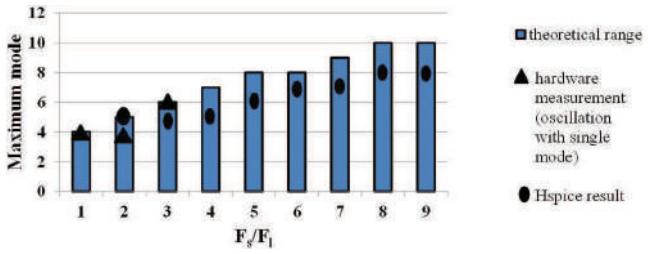


Figure 11. Possible modes for increasing F_s/F_l with simulation and experimental results superimposed.

The response function of rest of the linear portion comprises of cascaded transfer functions given by (7)

$$L(j\omega) = H(j\omega)Z(j\omega)S(j\omega) \tag{7}$$

Here S represents the discrete integration with sampling delay, Z represents ZOH and H is the plant transfer function. Evaluating (7) at $\omega_s/2n$ simplifies to

$$L(\frac{j\omega_s}{2n}) = \frac{e^{-j\frac{\omega_s}{2n}T}\angle - tan^{-1}(\frac{\omega_s\tau}{2n})}{j\frac{\omega_s}{2n}\sqrt{1+(\frac{\omega_s\tau}{n})^2}} \tag{8}$$

Using (6) and (8) in (1) gives

$$\frac{\frac{2M}{nT}\sum_{0^-}^{n^-} sin(\frac{2\pi}{2n} + \frac{180^o}{2n})}{Asin(\frac{\omega_s}{2n}t + \phi)} \frac{e^{-j\frac{\omega_s}{2n}T}\angle - tan^{-1}(\frac{\omega_s\tau}{2n})}{j\frac{\omega_s}{2n}\sqrt{1+(\frac{\omega_s\tau}{n})^2}} = -1 \tag{9}$$

Finally, the linearized response function is evaluated using (9) which gives the bound on F_s/F_l ratio for mode-n. As an example, mode-3 simplifies to

$$-tan^{-1}(\frac{\tau\pi}{3T}) - 60^o - 90^o + 30^o - \phi = -180^o \tag{10}$$

$$\frac{\tau\pi}{3T} = tan(60^o - \phi) \tag{11}$$

$$0 < \frac{F_s}{F_l} < 1.65; 0 < \phi < 60^o \tag{12}$$

Total feed forward gain per cycle is given by $K = K_{barrel}I_{pmos}$ and $\tau = 1/F_l$. Fig. 11 summarizes the accuracy of the obtained model compared with simulation and experimental results. The necessary range shows the presence or absence of a given mode for a F_s/F_l value. The dynamic range of experimental setup allows verification till F_s/F_l of 3. The above analysis can capture F_s/F_l bounds for any equivalent design changes in the feeback loop following the exact analysis presented in this section. These bounds represent the necessary conditions for a limit cycle to exist but may not be sufficient as amplitude condition in Nyquist criterion also needs to be satisfied. If multiple modes are possible for a given F_s/F_l value, then the exact oscillation mode is determined by the forward gain in the loop which is highly non-linear since a digital LDO output PMOS array is not biased as current sources but rather switches with low gain but small 'on' resistance.

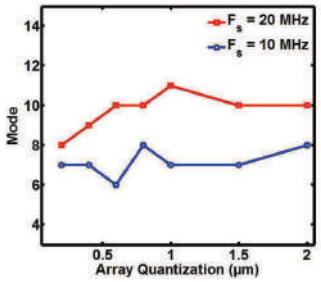


Figure 12. Lmit cycle modes with increasing PMOS array quantization at two different F_s.

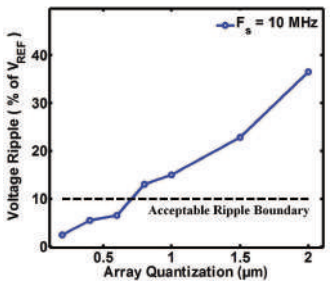


Figure 13. Increasing ripple with larger PMOS array quantization.

B. The Role of Quantization of the PMOS Array

The size of each PMOS in the array plays an important role in determining the overall forward path gain. It should be noted that an increase in the output ripple does not ncessarily cause an equivalent increase in the mode. Following the amplitude requirement imposed on the existance of a limit cycle by (9) an increase in I_{PMOS}, with larger size of each PMOS of the array, results in an increase in the forward path gain. This increases the V_{OUT} ripple even though the steady-state mode may only undergo negligible increase as verified by Fig. 12. Due to second order effects in $I_d - V_{sd}$ charactersitics of the PMOS array, the gain is non-linear and can be quantified through numerical simulations. Since there are a number of possible modes of oscillations, the exact mode of oscillation in which the loop settles down under given load conditions is a function of the forward-path gain. This trend is valid if F_s/F_l is not large. The overall array size is determined by the current requirements of the underlying load; whereas, the array quantization is set by the ripple specification. For the current design, a width of 750nm of each PMOS gives a maximum gain while remaining within the ripple bound at a maximum specified F_s/F_l as depicted in Fig. 13.

Similarly, increasing the capacitance at the output decreases output ripple but F_l decreases as well. This causes an increase in the mode of oscillation which may increase the steady state ripple. Although the two trends oppose each other but ultimately ripple changes the drop-out on the PMOS array which determines the forward gain. A lower ripple translates into an overall lower loop gain which prevents further increase in

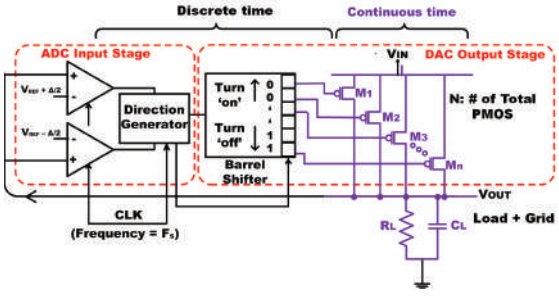


Figure 14. Proposed variant of baseline DLDO with dead-zone A/D converter, barrel shifter and a PMOS array.

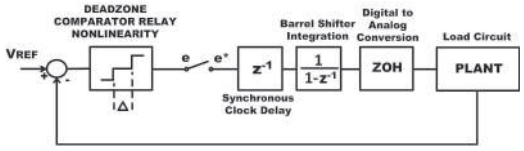


Figure 15. Steady state model for the digital LDO with deadzone.

the mode. It should also be mentioned that the overall DLDO loop presents two distinct quatizers. The first one is the input sampling stage, where a clocked comparator presents a hard quantization of the sampled input. The output stage, consisting of the PMOS array presents the second quantization. Since the number of quantization levels at the output is significantly higher than at the input, the quantization noise introduced at the input dominates the overall non-linearity in the loop. Hence, it is not surprising that the sampling frequency plays a significant role in the limit cycle dynamics, whereas the PMOS array has a less prominant role in determining the mode of limit cycle oscillations.

IV. DEAD-ZONE CONTROLLER FOR REDUCED STEADY STATE RIPPLE

The gain provided by the relay based nonlinearity is a function of both amplitude and phase of the input sampled signal. Decreasing this gain enhances the stability of the system which results in reducing or eliminating the limit cycle oscillations. This can be achieved by introducing a dead-zone in the comparator stage by using two comparators in tandem,

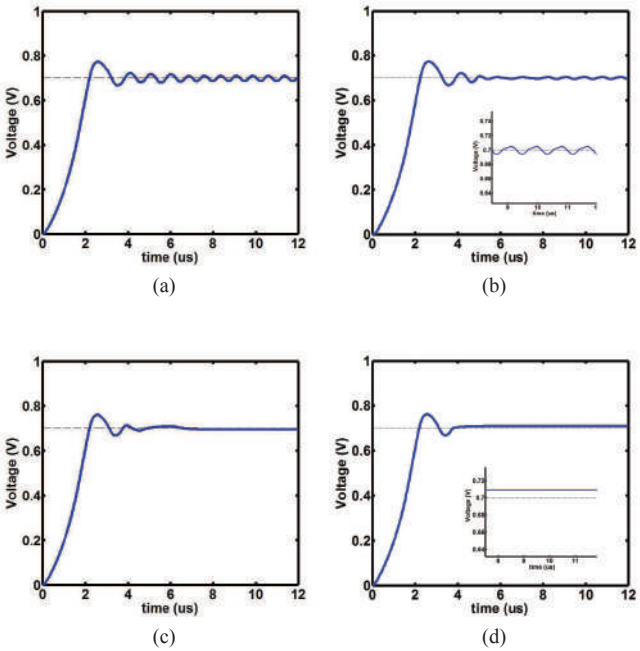


Figure 16. Increasing deadzone (a-d) removes steady state oscillations at the cost of the accuracy of DC regulation.

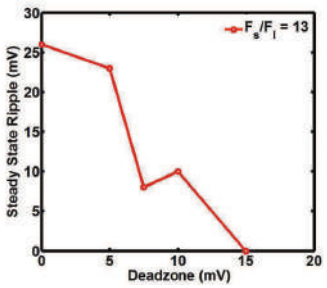


Figure 17. Trend of decreasing steady state voltage ripple with increasing deadzone.

followed by a shift logic block that produces the direction as well as a clock enable for the barrel shifter. Fig. 14 gives the detailed system level design of the deadzone DLDO. The two clocked comparators in the ADC stage can provide both a symmetric and non-symmetric deadzone around V_{REF}. Shift logic in the barrel shifter is temporarily disabled when V_{OUT} is within the deadzone. This not only helps in removing the steady state oscillations but also saves dynamic power consumed in a continuously clocked running barrel shifter. An equivalent steady state model, devised following the same procedure adopted before, is shown in Fig. 15. A relay with deadzone captures the steady state dynamics of the two comparator ADC stages. The summation of samples in (6) during the deadzone results in zero. Therefore, the forward-path gain is reduced as the size of deadzone increases ($K_{forward}\alpha 1/\Delta$). This helps to remove the limit cycle oscillations as illustrated by graphs in Fig. 16 and 17. However this limits accuracy of the DC load and line regulation, and the accuracy decreases for increasing the deadzone voltage. Thus the deadzone provides a design trade-off between the steady-state output ripple and the steady-state error (i.e., the difference between V_{REF} and V_{OUT}) and also acts as a powerful knob to increase current efficiency of the regulator under suitable load conditions where a bounded steady-state error may be tolerable.

V. Conclusions

A non-linear sampled feedback control model is proposed to model the limit cycle oscillations observed in discrete time digital LDOs. The model is validated through HSPICE simulations of a point of load discrete time digital low dropout (DLDO) regulator designed in a commercial 130 nm PDK. The results are further substantiated with hardware measurements of a representative prototype built on PCB with discrete components. The analysis comprehends the steady state dynamics of digital LDOs and ascertains the role of the sampling frequecny and the size of power MOSFETs (array quantization) in steady-state. A modification to the baseline design with a dead-zone controller is presented and analyzed to improve the steady-state performance of the DLDO.

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