Integrated Power Management in IoT Devices under Wide Dynamic Ranges of Operation

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Invited

ABSTRACT

By the year 2020 it is expected that corresponding to every human being there would be seven connected devices. These connected devices will usher in the Internet of Things (IoTs) and would percolate every aspect of human life, changing the human experience at a fundamental level. In order to power these devices novel strategies would have to be developed as these devices will not only have a dynamic load, due to multiple features, but also dynamic sources if opportunistic energy harvesting is used to supplement the rechargeable battery. For the power delivery network, figures of merit would be to comprehend both the ability to supply the worst case design as well as to maintain high efficiency across a wide dynamic range. To maintain high efficiency for a large range we will need adaptive components on the load side as well as at the energy source. In this work we will discuss the general IoT power delivery network (PDN), current research and the state of the art PDN components, novel designs and control for interface circuits and energy harvesters.

General Terms

Performance, Design, Theory

Keywords

Internet of things, Power delivery networks, Voltage converters, LDOs, Voltage regulators, Adaptation, MPPT

1. Introduction

Four decades of continuous scaling and the indisputable triumph of Moore's law have enabled a plethora of low power computation and communication devices. This has heralded a new generation of complex and compact devices that are influencing human civilization at a very broad scale. These devices have now permeated across our daily life and they manifest themselves in hand-held, wearable and implanted devices, cyber-physical systems and distributed sensor nodes that interact and share information. Due to the mobile and sometimes standalone nature of these devices, powering them poses a new paradigm in power delivery solutions. Due to ever increasing demand for features in these devices, the workload being executed demonstrate a huge variation in terms of both voltage and current. Further, to improve the battery life and due to the increased momentum in the field of ambient energy harvesting, opportunistic energy harvesters is also becoming a reality. This adds another dimension to the challenge, as energy harvesters are variable and sporadic sources of power.

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We need to provide a platform and interface circuits for optimum power transfer at minimum losses. Traditional power delivery networks designed for servers, desktops and high end mobile phones are based upon worst case load condition. This approach is targeted for performance and therefore is rendered handicapped in the IoT world where power-efficiency continues to play an ever-increasing role. Worst case designs are agnostic towards the wide scale variations both of load circuits (digital, analog and RF) as well as energy sources. Therefore it is critical to re-evaluate and modify the strategy for designing power delivery networks for IoTs. Adaptive and reconfigurable designs for components close to both source and load can be a viable and energy efficient solution. In this work we will discuss such adaptive designs and control strategies that can allow us to efficiently power the next generation of IoTs, amidst all the variations and dynamic conditions.

2. Power Delivery Networks for IoTs

2.1 The Source and the Load

Fig 1 shows a typical power flow architecture for a IoT device. The architecture consists of three important stages -- the source, the power delivery network and the load. In general the source is a rechargeable battery. Over the last few years there has been a resurgence of energy harvesting devices. This has been facilitated by two factor: (1) the energy conversion efficiency of the harvesting transducers are increasing at a rapid pace and (2) load circuits, particularly for IoTs are demanding lower and lower power thereby narrowing the gap between the supply (harvesters) and the demand (load). Some of the important energy harvesters include photovoltaic, vibrational, thermoelectric and wireless energy scavengers. The load can consists of variety of circuits and components depending upon the application. Digital Circuits could include CPU, GPU, memory, accelerators, audio and video processing blocks etc. There are also a number of analog and RF blocks that are quintessential for a connected world. In between the energy sources and the loads, we have a power delivery network whose primary task is to provide stability of the supply voltages,

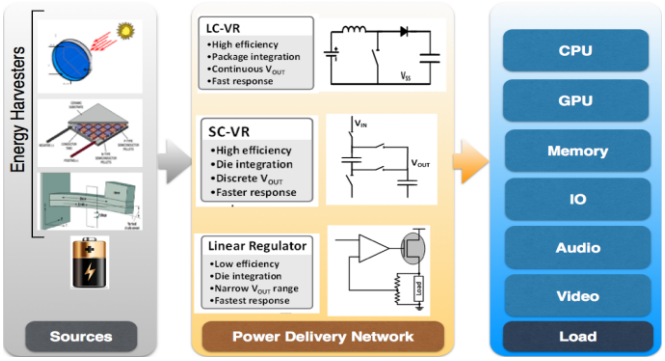


Fig.1: Power distribution Architecture in a typical IoT

high power efficiency, excellent load and line regulation as well as maximum power transfer from the source to the load in a highly dynamic and ever-changing environment.

2.2 Components of the PDN

Before going into the details of adaptive designs suited for large dynamic ranges, let us briefly discuss the various PDN components in a representative design. These components can be classified broadly into switching DC-DC converters and integrated linear regulators.

2.2.1 Switching DC-DC Converters

Switched inductor (SL) or switched capacitor (SC) converters are primarily used to step down high input voltage coming from secondary batteries to levels compatible with CMOS logic. The converters in general feed to a single voltage regulator in case there is only one power domain or can provide voltage and current to several voltage regulators in case of multiple voltage domains. Such converters operate in a feedback loop to stabilize the output voltage independent of the load current [8]. Although potentially both the SL and SC converters can be implemented on-die, each of these has its own unique challenge. SC converters have been demonstrated with on-die integrated capacitors, but they typically suffer from low capacitance density. Technology-circuit co-design has been explored in [9] to enable competitive SC converters. However, due to their limited applicability and cost (in terms of silicon area) we will restrict ourselves here to SL converters. In SL converters, the integrator is either on the PCB or in the package and provides significantly higher power density. It can convert voltage supplied by the battery (3.3-5V) to CMOS compatible levels (~1V), when operated to a buck or step-down mode. When operated to boost the voltage level (typically from a harvester) to either supply the load or to charge a secondary battery, SL converters operate as boost converters. Extensive work has been done for both boost and buck topologies and they continue to be the mainstays of the PDN.

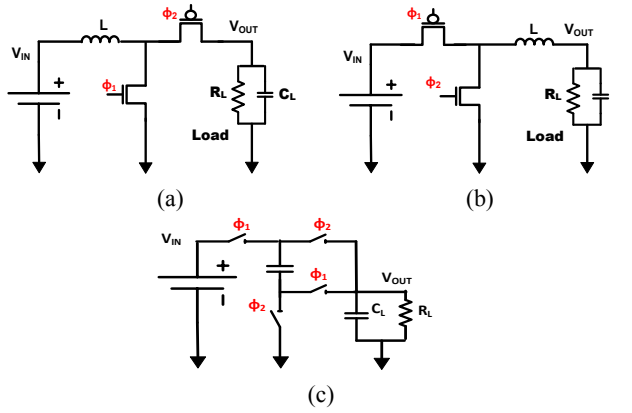


Fig. 2: Switching Converters: (a) SL Boost (b) SL Buck (c) SC

2.2.2 Voltage Regulators

The output of switching inverters have ripple, although advanced techniques like time-interleaving and multi-phased designs can alleviate a part of the problem. To supply a constant voltage to the load, and suppress any ripple, linear voltage regulators are the most popular design choices. As we move into a domain of ultra-fine grained spatio-temporal power management, linear regulators continued to be distributed across the die. Linear regulators provide regulation by dynamically changing the resistance of an active series resistor to maintain a constant voltage across the load. Hence, they are inherently lossy and can only be as efficient as V_{OUT}/V_{IN} where V_{OUT} and V_{IN} are the output and input voltages of the linear regulator, respectively. An important class of efficient linear regulators are low-dropout regulators (LDOs) whose drop-out voltage (V_{IN}-V_{OUT}) can be as low as 50mV. The last couple of decades have seen continuous improvement in the design, implementation and integration of analog linear regulators (including LDOs). They exhibit high load/line regulation, high bandwidth as well as high power supply rejection. However with continuous lowering of V_{IN}, analog linear regulators are losing their ranges of application. Research has started in earnest to supplement analog linear regulators with synthesizable, process and voltage scalable, all-digital linear regulators that have been demonstrated to enable fast response at extremely low controller currents [1]. Both analog and digital loops have been incorporated in [7] to provide high bandwidth as well as high energy efficiency.

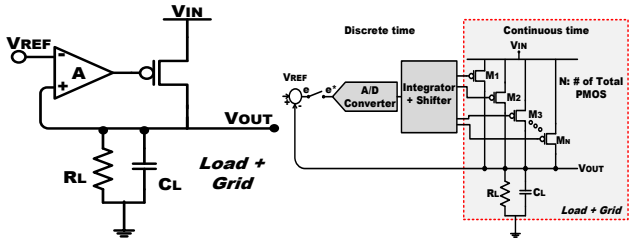


Fig. 3: Linear Regulator topologies: (a) Analog and (b) Digital

3. The Dynamic Source

In the last decade there has been continuous development in the area of low power devices and this is accompanied by significant improvement in the efficiency and the absolute power produced by energy harvesters. As the gap between the energy produced by harvesters and that demanded by load circuits keep on reducing, it is expected that self-powered IoTs will soon become a reality. In certain applications, fully self-powered systems may remain impractical, but opportunistic energy harvesting where the secondary battery is supplemented with energy harvesting will become feasible. These will be of significant application in distributed sensor nodes where many of these devices may be deployed and may remain physically inaccessible. It is important, however, to note that energy harvesters by their very nature are sporadic and suffer from extreme variations in the power output, depending upon the natural conditions that they are subjected to. The Thevenin model for every harvester in general demonstrates an extreme variation in terms of open circuit voltages, short circuit current and internal resistances. Table 1 summarizes some typical ranges of open circuit voltages and short circuit currents of three different harvesters [11-13]. These ranges can be further exacerbated through process, temperature and manufacturing variations. Combining the energy from multiple energy harvesters could serve as a powerful method to improve the IoT device battery-life and reliability as long as the PDN can deliver maximum transfer of power under such varying source conditions.

Table 1. Comparison of different energy harvesters in terms of open circuit voltage and short circuit current (Thevnin model)

Type of Energy Harvester	Open Circuit Voltage (V_{OL})	Short Circuit Current (I_{SC})
Photovoltaic	0.58-0.62 V	0.9-8.6 A
Thermoelectric	0.42-2.75 V	0.5-2.4 mA
Vibrational	4-12 V	0.1-0.29 mA

3.1 PDN (on the Source Side) Challenges

The PDN interfaces with these sources and plays two important roles. The PDN deals with a range of impendences of the energy harvesters with varying output powers, as seen in Table 1. In certain classes of harvesters, e.g., thermoelectric and vibrational transducers the output impedance of the harvester remains within a narrow range whereas for a photovoltaic, the driving point impedance exhibits a large dynamic range. The Maximum Power Transfer (MPT) theory states that in order to obtain maximum power the load resistance should be equal to the internal resistance of the source. In this case the load resistance is the effective resistance offered by the power delivery network's interfacing component. The second important role is to step-up or boost the voltage produced by the harvesters. As we note in Table 1, the output voltage of energy harvester could be extremely low, a few 100 of mVs and the load circuits may require higher voltages, typically ~1V. Both these roles could be played by an off-chip Boost converter design. In certain cases for example the vibration energy harvesters the voltage produced could be higher than required in that case and a buck-boost converter could be used.

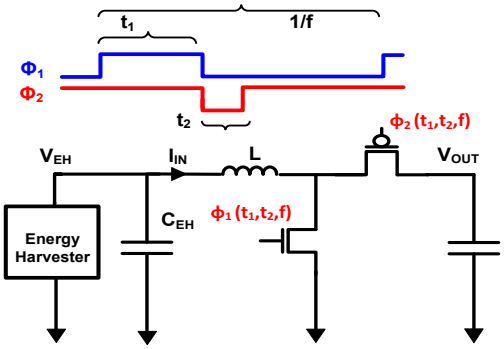


Fig. 4: Boost converter as interface circuit for an Energy harvester

3.1.1 Determining Optimal Impedance for Maximum Power Transfer and Boosting Ratio

Fig. (4) shows a boost converter that interfaces with an energy harvester and serves as the maximum power extractor. Let us consider a typical design to illustrate the key design challenges and solutions. In order to operate the boost converter at low power the discontinuous conduction mode is typically chosen. During the first switching phase, ϕ_1 the inductor charges to maximum inductor current for time t_1 and in the next phase ϕ_2 it charges down to 0 for time, t_2. After that there is a dead period where the inductor does not conduct any current as both the paths are cut off. It has been shown in [6], that the input resistance of the harvester (also the driving point impedance) can be modelled as by

$$R_{IN} = \frac{V_{EH}}{\langle I_{IN} \rangle} = \frac{2*L}{t_1*(t_1+t_2)*f} \approx \frac{2*L}{t_1^2*f} \quad (1)$$

Where f is the switching frequency and L is the inductance. The last part of the equation assumes that $t_2 \ll t_1$ which is generally true because the harvester may generally require a boosting ratio as high as 10x. The boosting ratio is

$$\frac{V_{OUT}}{V_{IN}} \approx \frac{t_1+t_2}{t_2} \quad (2)$$

This would also hold for buck-boost converters because the harvester provides power only in the first phase and charges the inductor. We could have considered the case of continuous conduction mode where $t_1 + t_2 = {}^1/_f$ but that would reduce one of the knobs (degree of freedom) at our disposal for modifying the input resistance as shown here

$$R_{IN} = \frac{V_{EH}}{\langle I_{IN} \rangle} = \frac{2 * L}{t_1}$$

3.2 Static vs Dynamic PDN for sources

To extract the maximum power from a harvester, the looking-in impedance (resistance), R_{IN} provided by boost converter needs to be equal to the internal resistance of the energy harvester. This is critical when we are using multiple energy harvesters because different harvesters will have different output impedances. While a static network would not be able to handle multiple energy harvesters a adaptive PDN can utilize the boost converter (or buck-boost converter) and offer a suitable impedance by changing either the switching frequency or the time interval, t_1.

Now consider the case where the same energy harvester operates at different voltage levels due to static and dynamic variations. When faced with different voltage levels the designer can choose to allow the boosting ratio to remain same in a static design, but this can have significant implications on the system efficiency, particularly when the dc-dc converter is followed by a linear regulator (in LDO mode) with a large drop-out. The theoretical maximum efficiency an LDO can provide is the ratio of regulated voltage and the input voltage of the LDO and is given by:

$$\eta = \frac{V_{OUT,LDO}}{V_{IN,LDO}} * \frac{I_{LOAD}}{I_{LOAD}+I_{Control}} \quad (3)$$

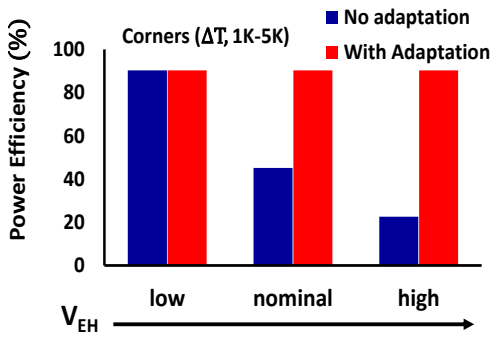


Fig. 5: Power efficiency degradation as a function of the output power of the energy harvester (V_{EH}) when the PDN is designed for the worst case

The second ratio (the ratio of currents) is called the current efficiency of the LDO. Let us consider an example. As shown in Fig. 5, we consider a thermoelectric energy harvester with a static dc-dc converter. The design assumes worst case corner so the assumption is based on the fact that the thermoelectric energy harvester is a producing a low open circuit voltage of ~0.05 V. However during nominal usage the output voltage could assume that the load current delivered by the harvester is constant. If the boosting ratio of the dc-dc boost converter is kept constant and the voltage demand on the load circuit is unchanged, any extra voltage generated by the boost converter must be dropped across the LDO. This leads to significant energy loss in the system. Alternatively, an adaptive design would be able to adjust the boosting ratio to minimize losses across the PDN. Our calculations show that when the harvester delivers high power and voltage the system-level power efficiency drops to 23.75% and in nominal mode of

operation it is slightly lower than 50%. Hence a worst case, static design cannot fully comprehend the opportunities presented by a dynamic environment and an adaptive PDN can reduce a loss of pessimism in design.

One simple circuit level solution to improve this drastic drop in energy efficiency is to change the boosting ratio by changing t_2 and keeping $t_1 + t_2$ constant. The control circuitry required would have a feedback system which constantly monitors the output voltage keeps increasing t2 until the boosting ratio is meets a target. Details of this design can be found in [6]. Alternative design styles can also be adopted, as long as adaptation to the dynamic environment is sensed and the PDN adjusted based on the current supply and demand constraints. Utilizing this technique would ensure that the high efficiency is maintained across the large dynamic range of V_{EH}. This has been shown in the bar-chart of Fig. 4 through the with adaptation bars.

3.3 Adaptation towards Variation of Passives

One of the key drivers in the widespread deployment of IoTs is expected to be cost. On package, PCB and on-die passives increase system cost and often their quality and tolerance are compromised for lowering system cost. We continue to see large variations in the performance of passives and often they degrade very sharply over time. For example, in buck/boost converters, we note large variations in the inductance offered by the inductors and also, the value of the inductance degrade over time. A key challenge is to maintain efficient power management in spite of such variations and dynamic changes related to aging.

As an example, let us consider same thermoelectric energy harvester with a boost converter whose self-inductance degrades with aging. The simulated data demonstrates that with 50% degradation of L there is 15% reduction in the output power when all other factors (trace resistances, boosting ratios and control dynamics) are kept constant. Fig 6 represents the ratio of output power to the possible maximum power that can be extracted, versus percentage degradation of the inductance with time.

This can be fixed either by an adaptation where either the frequency or t_1 is modified (appropriately) to offer appropriate matching impedance.

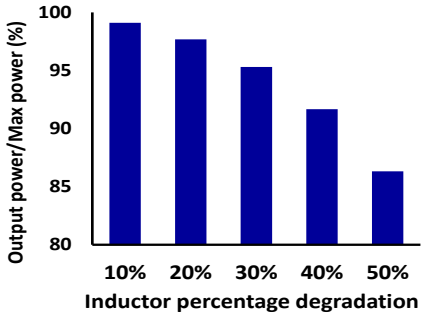


Fig. 6: Extracted power reduction in a static PDN due to Inductor degradation

3.4 MPPT for Photo-voltaic (PV) Sources

So far, we have discussed thermoelectric harvesters. Let us now explore photo-voltaic harvesting devices. The I-V characteristics for photovoltaic sources have been shown in the Fig. 7**.** Unlike other energy harvesters PV cells contain non-linear elements. The I-V relationship is not linear; therefore, a one-time calibration of the internal resistance for PV harvesters is insufficient. Instead it would require the design to monitor the available power conditions and through feedback and maximum power point tracking (MPPT). In most of the cases volt-meters or current-meters can be used to estimate the available power.

In [10] where a Zero Crossing Scheme for the inductor current is used to estimate the power output of a PV harvester. It has been shown that for maximum power transfer,

$$t_2 = \sqrt{\frac{2L * P_{extracted}}{V_{OUT}(V_{OUT} - V_{EH})f}} \quad (4)$$

Therefore in a discontinuous conduction mode as t_2 increases the extracted power also increases.

As shown in the Fig. 8 through a one bit feedback signal that compares V_{MID} to V_{OUT}, t_2 pulse-width is either incremented or decremented. Eventually this should lead to the required pulse-width for zero current switching.

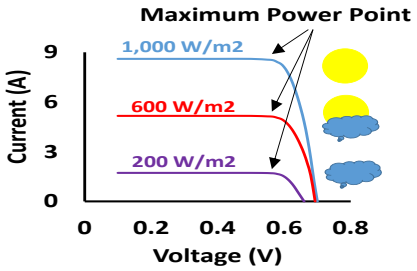


Fig. 7: I-V characteristics of Photovoltaic Energy Harvester

Once we have a measure of power through t_2 we can vary a number of control parameters that can modify the impedance offered by the boost converter. We can use either t_1 or the switching frequency to obtain the Maximum power point.

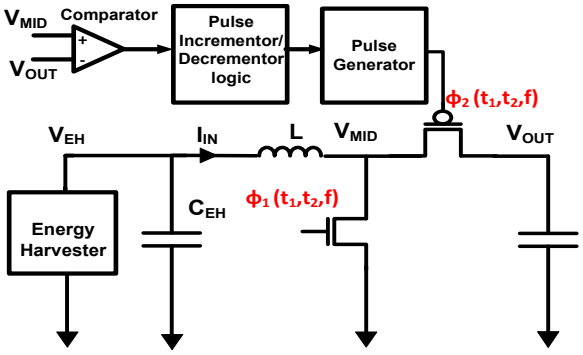


Fig. 8: Measure of t_2 through Zero Crossing Scheme [10]

4. The Dynamic Load

To achieve high power efficiency without sacrificing performance the loads circuits employ dynamic voltage and frequency scaling. Also, fine-grained clock and power gating are used to minimize power consumption in the unused domains of the load circuit. Further, due to consistent increase in the demand of features the workload varies in time. Changes in temperature and aging can cause changes in the load current ranges both spatially as well as in time. Considering that the IoTs would need to be economically designed, low cost packaging adds variations and further increases the load current ranges. A typical core in a normal processor can demonstrate current variations from a few A to a few µA. A simple

smart watch, for example, can demonstrate current ranges from 50-100 mA to a few µAs. So modern PDNs not only need to supply voltages across multiple operating voltages but needs to supply large ranges of current with high stability, low ripple, fast response times and low line/load regulations.

4.1 Static LDO (Load Side) Design Challenges

On-Chip Integrated low drop out voltage regulators (LDO VRs) are widely used to provide consistent and well-regulated voltage to the load circuits. On-Chip LDO VRs play a critical role by stepping down the noisy input voltage and providing a clean supply to the loads. The LDOs are fast and are their integration at the chip level is well understood. However the LDOs power efficiency is dependent on two crucial components as showing in the equation 3. It is directly related to the ratio of V_{OUT} to V_{IN}. So the higher the dropout (V_{OUT} - V_{IN}) the lower the maximum efficiency possible. Another component that adds to this is the current efficiency. At higher load values the controller current of the digital LDOs is insignificant and it is nearly equal to one. However, during the light load scenarios the controller current can become a significant portion of the overall current and lower the net efficiency. This renders the traditional static design of LDOs pessimistic. Current research addresses this problem by allowing the control loop of an LDO to adapt and change itself depending on the load current and operating conditions.

Apart from the loss of efficiency due to the extremely large current ranges, another important design criteria is the loop stability. The LDO loop needs to be stable amidst large changes in the load current. It can be qualitatively understood, that changes in the load current would result in changes in the output pole position of the LDO loop (a larger load current would push the output pole to a higher frequency). Even for a well-compensated loop, it is often difficult to achieve high phase/gain margin for a 100x change in the load current (and hence the load pole position). This requires adaptation – changes in the loop characteristics depending on the output current and the output pole position. This removes pessimism, addresses the issues of worst case design and can guarantee high efficiency and stability across a 50-100x load current range.

Such adaptive design techniques have been studied for both analog as well as for digital linear regulators. We will discuss both these design techniques very briefly here and the interested readers are pointed to [1],[2],[14] for further discussions.

4.2 Adaptive Control in LDOs

Fully Analog LDO: One of the recent articles on the use of adaptive control in analog LDOs is [14]. It features adaptive RC compensation and current boost networks controlled by load sensors to provide quality of power control and optimization. The compensation network comprises of a capacitive block connected in series with two resistive blocks. These resistive blocks are digitally controlled and are configured to stabilize the LDO under a wide range of load current variations.

The Fig.9 shows the adaptive compensation block schematic which uses for a programmable RC network to adapt according to the load. Fig 10 demonstrated that through adaptation a phase margin higher than 40 degrees is maintained across a 10X current range. Interested readers are pointed to [14] for further discussion on the design.

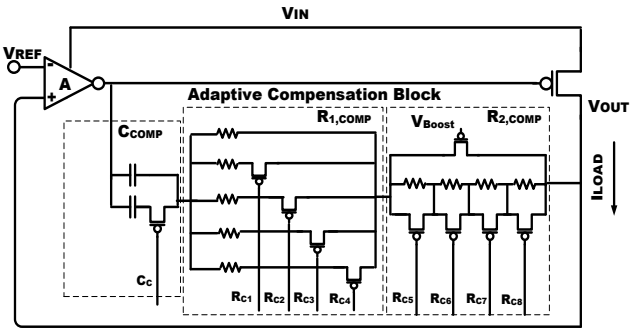
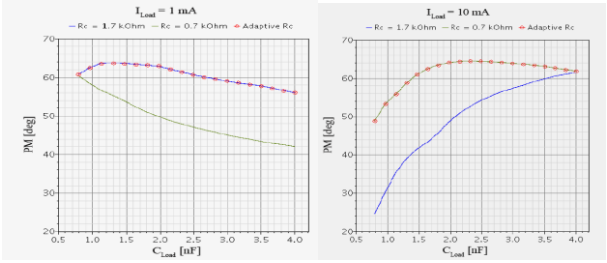


Fig. 9: Adaptive compensation block for Analog LDO [14]



(a) (b)

Fig. 10: Phase margin with different compensation and load capacitance (a)I_{LOAD} = 1mA (b) I_{LOAD} = 10mA. Plots reproduced from [14] with permission.

Fully Digital LDOs: In previous work from our group [1, 2] we demonstrated a fully digital LDO featuring adaptive control under wide range of operation. The design is based on a discrete time, fully digital, scan-programmable LDO macro designed in IBM 130nm CMOS technology. The design consists of a 128 bit barrel-shifter that control 128 identical P-MOSFETs to provide load and line regulation at output node. The digital utilizes a clocked sense amplifier based comparator, which does not use any bias current, compares the regulated voltage with a reference voltage and according to the result either increments or decrements the total number of PMOSs supplying the current. The total number of shifts in one shot is programmed through a gain K which could be either set to 1,2 or 3. It has been shown in [1] and [2] that a linearized control model of the LDO reveals two open loop poles (a) an integrator pole at z=1 and (b) $z = e^{-\frac{F_{LOAD}}{F_S}}$ where F_{LOAD} is the output (or, load) pole frequency and F_S is the sampling frequency of the controller. As the load current varies across several orders of magnitude (~100X) the open loop poles and consequently, the closed loop poles of the system go through a large dynamic range. This can lead to the system changing its behavior from over-damped (heavy load) to oscillatory system (light load). The key adaptation policy is to limit the output pole movement and this is done by varying the sampling frequency. The goal is to keep the ratio $\frac{F_{LOAD}}{F_S}$ within bounds. By sensing how many P-MOSFETs are required to supply the current a good estimate of the load current can be made and the sampling frequency can be appropriately modified. Such an adaptation scheme has two advantages: (a) it bounds the position of the closed loop system poles and hence provides a more consistent and stable response even under wide dynamic range of the load currents; and (b) by slowing down the sampling frequency at light load conditions, the controller power scales with the load current and hence maintains high current efficiency across a large range of operation. Fig. 11 illustrates the improvement in current efficiency in a digital LDO with adaptation.

Here, Adaptation is achieved by adapting the sampling frequency, F_S with load current, as seen in Fig. 12(a). We also note that to achieve the same settling time, T_S, at different load conditions, we need to adapt F_S with load current. This has been shown in Fig. 12(b).

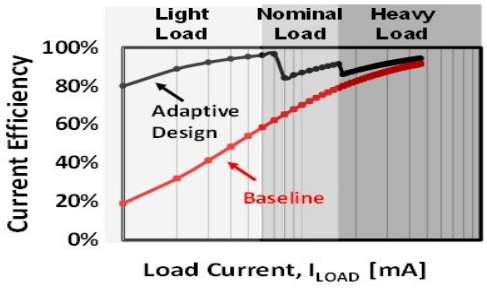
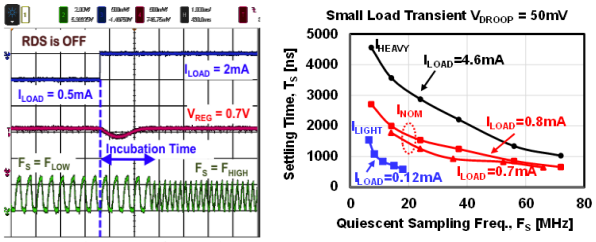


Fig. 11: Current efficiency in Digital LDO with and without adaptation



(a) (b)

Fig. 12: (a) Demonstration of switching frequency adaptation according to the load current changes (b) Measured settling time, T_S (for small droops) show a wide F_s range for iso-T_S at nominal conditions

5. Concluding Remarks

As power management becomes an ever-increasing concern in the IoT space, the demands from the DC-DC converters and integrated voltage regulators keep on increasing. Through representative power delivery architectures and designs, we have shown that both the sources and the loads are highly dynamic and go through large dynamic ranges. The well-established methodologies of a static or worst case based PDN design will not provide optimum solutions any more. We need a dynamic and adaptive PDN which will transfer power from the source to the load with maximum efficiency. This needs to be done under constraints of performance, load and line regulation as well as stability. We have shown examples of analog and digital regulators and converters where adaptive design principles have been used with large improvements. We need further improvements in PDN technologies, better CAD tools and hardware designs that will perform co-optimization of PDN components with the load and sources. This will allow improvements in system level efficiencies, robustness towards variations and tolerance towards low-cost, variation prone package components.

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