

A Time Interleaved DAC Sharing SAR Pipeline ADC for Ultra-Low Power Camera Front Ends

Anvesha Amaravati, *Student Member, IEEE*, Manan Chugh, Arijit Raychowdhury, *Member, IEEE*,
School of Electrical and Computer Engineering, Georgia Institute of Technology.
email: {aamaravati3, manan.chugh}@gatech.edu, arijit.raychowdhury@ece.gatech.edu

Abstract—The growing need for ultra-low power cameras for sensors, surveillance and consumer applications has resulted in significant advances in compressed domain data acquisition from pixel arrays. In this paper we present a novel 64-input Successive Approximation (SAR) Pipeline analog-to-digital converter (ADC) suitable for compressed domain data acquisition in camera front-ends. The proposed architecture features a time interleaved capacitive digital-to-analog converter (DAC) shared between column parallel ADCs for area savings (2.28X); and a shared amplifier stage for power savings (60%). Simulations on a 130nm foundry process shows that the proposed SAR Pipeline ADC draws $31\mu\text{W}$ at 2MS/s having a target Figure-of-Merit (FOM) of 87fJ/conv. per step at Nyquist rate.

Keywords—DAC sharing, SAR Pipeline, Compressive sensing.

I. INTRODUCTION

Wearable devices for IOT (Internet of Things) require CMOS image sensor (CIS) with low power and area [1]. Traditional CIS for wearable devices consume power more than 50mW[2]. In a CMOS image sensor system column parallel ADCs along with digital processors consume most of the power[3][4]. In most of the reported image sensors, column parallel ADCs draw 50-65% of the power of the entire image sensor chip[5][1]. The power consumed by column parallel ADCs is proportional to the number of measurements to be performed by the ADC. It increases with the number of pixels. Cameras used in surveillance, continuous time monitoring, human machine interfaces etc., need to be “always on” and low-power is regarded as a key enabler for such next generation IoT devices.

Recently developed algorithms of compressive sensing (CS) promise to reduce the number of measurements with non-linear recovery at the back-end [6]. If the pixel values in a camera are represented as a discrete time signal $X = [x_1 x_2 x_3 x_4 \dots x_n]^T$, the number of measurements needed in traditional column parallel ADCs will be equal to n . Instead of n samples, CS needs only m linear measurements ($m \ll n$). The CS measurement matrix is given by Eq. 1.

$$Y[m] = \phi[m, n] \times X[n] = \begin{pmatrix} 0 & 1 & \dots & 1 \\ 1 & 1 & \dots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 1 & 0 & \dots & 0_{m,n} \end{pmatrix} \times \begin{pmatrix} x_1 \\ x_2 \\ \vdots \\ x_n \end{pmatrix} \quad (1)$$

Here $Y[m]$ is the m -dimensional measured array, ϕ is a random binary matrix of size $m \times n$ and follows the “Independent and Identically Distributed (IID)” property. X is traditionally recovered at the back-end using an optimization algorithm, like determining the L_1 norm[6].

In this paper we present a novel pipeline-SAR ADC architecture with capacitive DAC sharing with the capability of acquiring linear combinations of 64 pixel data in a single conversion cycle. This is suitable for such compressed domain data acquisition.

II. ADC ARCHITECTURES FOR CS IMAGE ACQUISITION

In prior work for obtaining compressed domain data, both analog and digital techniques have been used to perform compressive measurements from the raw data. Typically, analog implementations of compressive sensing suffer from low Signal to Noise Ratio (SNR) and require an analog to digital converter to improve accuracy[7][8]. Resistor based compressed sensing multiplexor reported in [9], suffers from static power dissipation and the number of inputs (n) is limited, making it suitable for RF receiver applications only.

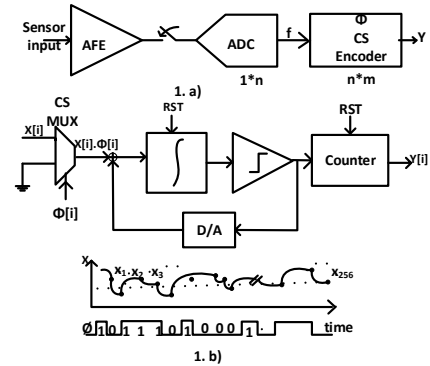


Fig. 1. a) CS encoder on acquired samples of ADC[10] b) Simultaneous compression and quantization within [5]

To overcome some of the disadvantages of analog CS circuits, [10] has proposed compression in the digital domain. Fig. 1. a) shows the technique proposed in [10]. The entire analog signal is converted into the digital domain by high-speed ADCs and the CS encoder does compression in the digital domain. This is mostly suited for bio-medical applications where the number of input channels are limited. However, for CIS of a typical 256×256 size, ADCs would need to acquire all

the samples and then convert to the digital domain. The number of measurements by the ADC will not be reduced and it defeats the purpose of compressed domain data acquisition. Further, the size of digital CS encoder grows exponentially with the number of inputs. CS encoders will further add significant power along with the ADC making it infeasible for “always on” imaging applications.

To overcome the limitations of data acquisition followed by compressed domain measurements, Oike et.al, has proposed a CS camera through simultaneous averaging and quantization of pixels using a $\Sigma - \Delta$ ADC [5]. Fig. 1. b) shows the schematic of the resetting $\Sigma - \Delta$ ADC used for such linear measurements. Pixel values are multiplied with random numbers (from the ϕ matrix) sequentially and passed to the input of the $\Sigma - \Delta$ ADC. This approach requires m measurements; however it requires n conversion cycles for one measurement. This architecture requires a $16 * 16$ block for linear measurement. For each measurement of the block, the resetting $\Sigma - \Delta$ ADC needs 256 clock cycles. During this conversion period, all the high gain amplifiers will remain on and consume power. Hence, for lowering the total power dissipation, faster conversion with the opportunity for power gating once the conversion is complete, will be critical.

Once compressed domain data is acquired, the image is often used for online classification to detect potential trigger signals. For such in-situ classification [15] and trigger identification, 8bits of inputs are sufficient. Further, it has been shown that for most of the machine learning applications moderate resolution (6-8bits) is sufficient[1][11]. Fig. 2 shows the Energy per conversion with respect to the Signal to Noise and Distortion ratio (SNDR) for state of the art SAR, Pipeline and $\Sigma - \Delta$ ADCs. SNDR is related to effective number of bits ($ENOB = SNDR - 1.76/6$) [18]. From this plot we can observe that SAR ADC has best FOM (order of $10 - 1000 fJ/conv$) for moderate resolution (6-8 bits). Pipeline ADCs also have competitive FOM for moderate and high speed applications. Since most of the image sensors speed varies from 1MS/s to 10MS/s and we are interested in 8b of resolution for in-situ image processing applications, we propose a SAR-Pipeline ADC which achieves ultra-low power and high area efficiency.

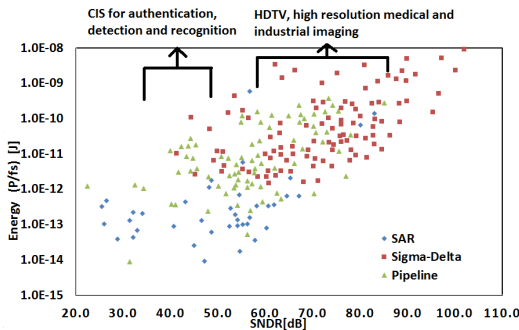


Fig. 2. Energy vs SNDR for state of the art reported SAR, Pipeline and $\Sigma - \Delta$ ADCs[14]

III. SAR-PIPELINE ADC ARCHITECTURE FOR CS MEASUREMENTS

For most of the low power applications SAR ADCs are used since they consume ultra-low energy per conversion (Fig. 2). But they are limited to low sampling rate & low resolution because of the DACs settling time for conversion (mainly set by MSB transition)[19] and large capacitance (for higher resolution). To alleviate this problem two-stage SAR Pipeline ADCs are proposed[19][20]. SAR-Pipeline uses two stage SAR-ADC and an amplifier which is used for amplifying residue generated by stage 1 SAR ADC (Fig. 3). Both the SAR ADC stages operates in parallel and each stage has to resolve lesser number of bits (lesser DAC settling time & capacitance as compared to traditional SAR). Therefore, SAR-Pipeline ADCs can operate at much higher speeds with high area efficiency [20]. One of the inherent advantage of SAR-Pipeline is residue voltage of Stag-1 SAR ADC is generated within its DAC after conversion phase. Hence this avoids extra DAC and clock phase to generate residue of Stage-1 unlike in traditional flash based Pipelined ADCs[20].

Fig. 3 illustrates the proposed ADC architecture. The design operates on a block size of $16 * 16$ (256 elements in pixel array). We propose SAR-Pipeline ADC consisting of 64-inputs Stage-1 SAR ADC resolving 4 bits (with 1bit redundancy) and Stage-2 SAR ADC resolving 5 bits. We propose time-interleaved DAC sharing for Stage-1 SAR ADC which provides a linear measurement of 64-inputs in a single cycle. We also share the amplifier (used for residue amplification) between 2 neighboring column parallel ADCs to save power. 64 inputs are simultaneously averaged and quantized using the SAR-Pipeline ADC. Post-conversion, 4 consecutive samples are averaged using a 10 bit accumulator and shift register. This allows us to average 256 samples in 4 sampling cycles.

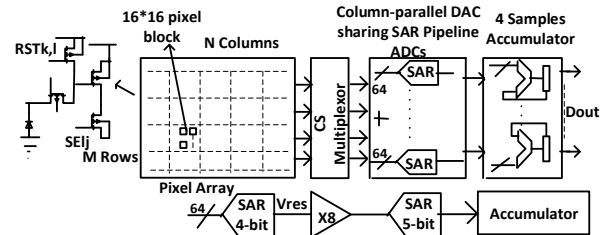


Fig. 3. Proposed CS front-end architecture for CIS

Fig. 4 shows a previously reported multi-input SAR ADC used for compressed sensing (with 8 bit resolution). It uses charge sharing. The MSB capacitor is equally divided among the inputs. Because of charge sharing the inputs will get averaged after the sampling cycle. [16] demonstrates a 4 input CS SAR ADC for wireless applications. This technique requires $(2^8 + 2^4 = 272C)$ number of capacitors for an 8 bit ADC and measures 256 inputs (C is the unit capacitor). One of the main limitations of the proposed SAR ADC architecture for portable application is the area occupied by the sampling capacitors[17]. Dividing the MSB capacitors to accommodate 256 inputs requires 256 switches. For portable applications

limited supply $\approx 1 - 1.3V$ provides high R_{ON} . This provides us the time constant (τ_{conv}) for conversion (min. sized capacitor of 50fF) of $\approx 220\text{nsecs}$ (DAC settling time). This allows a maximum sampling frequency of 730KHz. Hence, for high speed cameras (with 30frames/sec) the proposed ADC architecture will not be able to meet latency requirements.

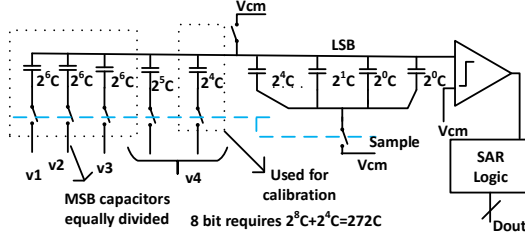


Fig. 4. Reported multi-input SAR-ADC[16]

Fig. 5 is the proposed SAR-Pipeline with DAC sharing. We use 4 bit ADC as the first stage. Since 4-bit ADC has 16C capacitors, all the capacitors are divided into equal value of C and 16 inputs are applied. We have 3 instances of the same DAC which is used for accessing additional 48 inputs. Sampling is done in two phases. During sampling phase (S1) all 4 DAC's sample 16 inputs each. During second phase of sampling charge is redistributed between them. The averaged voltages across 4 DAC's during S1 phase given by Eq. 2.

$$\begin{aligned} V_{dac1} &= \frac{(v_1 + v_2 + \dots + v_{16})}{16} \\ &\vdots \\ V_{dac4} &= \frac{(v_{48} + v_2 + \dots + v_{64})}{16} \end{aligned} \quad (2)$$

During the second sampling phase S2, averaging of V_{dac1} to V_{dac4} takes place. Therefore, the final voltage across DAC is given by Eq. 3.

$$\begin{aligned} V_{dacf} &= \frac{(V_{dac1} + \dots + V_{dac4})}{4} \\ V_{dacf} &= \frac{(v_1 + \dots + v_{64})}{64} \\ V_{dacf} &= \frac{(X[0].\phi[0] + \dots + X[63].\phi[63])}{64} \end{aligned} \quad (3)$$

We can observe from Eq. 3 that the final accumulated output represents the dot-product of the input pixel vector X with the sampling matrix, ϕ . ϕ can be random or programmed so that both random as well as structured compressed measurements can be obtained. As soon as S2 is done 3 DAC's are shared with neighboring column parallel ADC. Once the conversion in 4-bit SAR ADC is complete, we amplify the residue by 4x and pass it to a 5-bit fine ADC to resolve the LSBs. Ideally a gain of 16 is required for residue amplification. We use 1-bit digital redundancy in Stage 1 and half reference scaling for Stage 2 to reduce the gain requirement which helps to reduce the power in the high-gain op-amp [19].

Since all the capacitors we use are identical and of value C, calibration is not required (more details in section III). As 3 DAC's are shared with 4 ADC's, we need an additional capacitance of 12C. With 12C extra capacitance we can acquire

linear measurements of 64 inputs in each conversion cycle. This DAC shared method significantly improves area efficiency and enables simultaneous acquisition of multiple inputs. In this architecture, the conversion time-constant (τ_{conv}) is determined by the 4-bit ADC settling time even though we are sampling 64-inputs. This makes the architecture suitable for high speed sensing with large number of inputs.

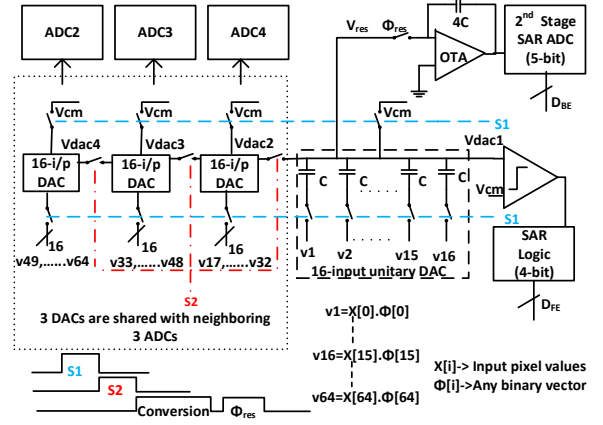


Fig. 5. Proposed multi-input DAC sharing SAR ADC

Fig. 6 shows how the sampling schemes are time-interleaved for the entire column parallel ADC architecture. Conversion cycle for ADC is 8 clock cycles. During this period we share 3 DACs with 3 of the neighboring ADCs. S3 to S8 are sampling phases of ADC2 to ADC4. S3 to S8 phase operates during conversion period of ADC1. Pipelining facilitates overlapping of Stage-1 and Stage-2 conversion phases. 1-bit redundancy is added in the first stage to accommodate capacitor mismatch and offsets of the comparator, amplifiers[19]. We also share residue amplifier between two neighboring ADCs to reduce the total power[20]. Accumulator (10 bit) used to average 4 consecutive ADC output samples. The accumulator is reset after every 4 sampling cycles (F_s). The sampler operating at quarter sampling rate is used to capture the averaged output. Fig. 6 also shows the control logic used for proposed CS front-end ADC architecture. Global reset (RST) is used generate S1, S2 and conversion phase for ADC1. S2 phase of ADC1 is used to trigger sampling phase for neighboring column parallel ADC. This process is continued for all 4 ADCs.

IV. DESIGN COMPONENTS

In this section, the design details of the first and the second state of the ADC are discussed.

A. Stage 1 ADC and residue amplification

Fig. 7 shows the Stage 1 of the proposed SAR-Pipeline ADC. 64 inputs are acquired from S1 and S2. Residue is fed into an amplifier with gain of 4. Stage 1 of the ADC has 4 bit resolution with 1 bit digital redundancy. 1 bit redundancy is used to accommodate the residual offset of the comparator, op-amp and capacitor mismatch errors.

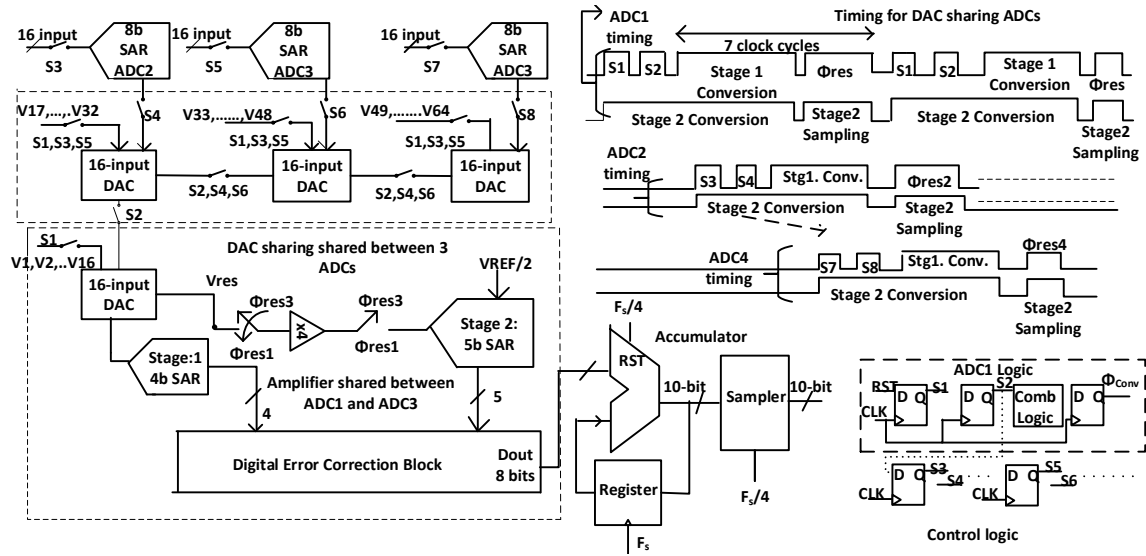


Fig. 6. Proposed SAR ADC with time-interleaved DAC sharing

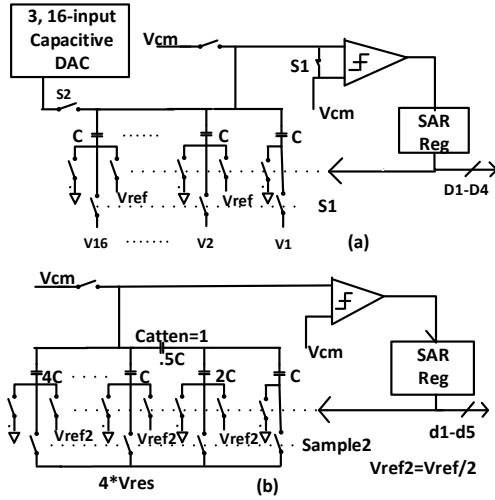


Fig. 7. Stage 1 and Stage 2 of the proposed ADC

The Op-amp open loop gain (A_{OL}), unity gain frequency (f_u) and swing ($V_p - p$) target based on the inter-stage gain is given in Table. I. The Target values are derived as per gain error, gain bandwidth (GBW) requirement of the OTA to be within 1/2LSB of the ADC error[20]. Simulated values across process corners are much above the Target values.

Inter-stage gain	Op-amp			2nd stage SAR
	A_{OL}	f_u	$V_p - p$	Offset
Target	42dB	42MHz	250mV	16.125mV
Simulated values	50dB	80MHz	300mV	8mV

TABLE I. DESIGN REQUIREMENT FOR AMPLIFIER AND 2ND STAGE OFFSET

We use pre-amplifier with output offset compensation to

limit the offset of Stage 1 SAR ADC. The residual offset ($V_{os,res}$) is given by Eq. 4.

$$V_{os,res} = \frac{V_{os,pre-amp}}{A_p} + \frac{V_{os,latch}}{A_p} \quad (4)$$

where $V_{os,pre-amp}$ and $V_{os,latch}$ are the pre-amplifier offset and latch offset respectively. A_p is the pre-amplifier gain. The 3σ $V_{os,pre-amp}$ and $V_{os,latch}$ are 5mV and 30mV respectively. The gain amplifier features a cross coupled load which provides a high gain of 15. The residual offset is 2.33mV which is 0.25LSB of the sub-ADC.

We use telescopic cascoded OTA in the proposed design for residue amplification. Telescopic cascoded OTA has high power efficiency for a given gain bandwidth (GBW)[18]. Because of half gain and half reference implementation of the ADC, the open loop gain of the OTA is reduced. The OTA achieves a swing of $300mV_{p-p}$.

B. Stage 2 ADC

Fig. 8 shows the Stage 2 of the proposed SAR-Pipeline ADC. We use a split capacitor architecture to reduce the area and power for the second ADC. Since the non-linearity of this ADC will get divided by the gain of the amplifier, it can be neglected. For the comparator in stage 2 of the proposed ADC, a pre-amplifier with gain of 3 is used since the offset requirement from it is 15mV. The total capacitance from the second ADC is 11C.

V. ANALYSIS OF CAPACITOR MISMATCH

Systematic variations has no effect of capacitor matching since all the capacitance in Stage 1 SAR ADC are equal to C. The capacitance mismatch standard deviation for metal-insulator-metal (MiM) is given by Eq. 5.

$$\sigma_{\Delta C/C} = \frac{A_{\Delta C/C}}{\sqrt{WL}} \quad (5)$$

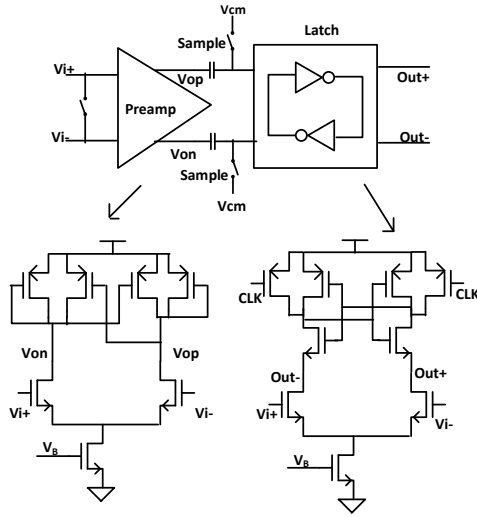


Fig. 8. 6-bit split cap SAR-ADC for Stage 2

where $A_{\Delta C/C}$ is process constant which is $1\% \cdot \mu m$ for $0.13\mu m$ CMOS process[21]. W & L are width and length of the capacitor. The minimum size allowed in $0.13\mu m$ is $5\mu m \times 5\mu m$. With minimum sized capacitor $\sigma_{\Delta C/C}$ obtained will be 0.002.

As per [22] maximum allowable capacitor mismatch for a resolution of n is given by Eq. 6.

$$\frac{\Delta C}{C_{max}} = \frac{2^n}{2^{2n} - 2^n + 1} \quad (6)$$

For $n=9$, $\Delta C/C_{max}$ reaches close to 0.002. This shows the residue generated by first ADC will fall within the range of $1/8LSB$ of error. Hence the proposed architecture is robust towards capacitor mismatch.

VI. SIMULATION RESULTS

Performance of the proposed SAR-Pipelined ADC is verified through design and simulations in the IBM $0.13\mu m$ CMOS.

Fig. 9 shows the normalized output frequency spectrum of the proposed ADC for input frequency (F_{in}) of 248.34kHz at sampling rate (F_s) of 1MSPS. A 1024-point FFT shows SNDR of 49.5dB which is equivalent to an ENOB of 7.9 for full scale input (dBFS). Fig. 10 shows the 64 inputs applied to ADC at each sampling cycle. Each 64 inputs corresponds to CS multiplexor output (Product of input vector with random number). Fig. 11 shows the ADC and accumulator outputs at each conversion cycles. For a particular case study, as shown in the figure, an ideal averaging without quantization results in a output of 270.11mV. The proposed ADC after accumulated 4 samples each provides an output of 269.53mV which is less than 1LSB of error. Fig. 12 shows the SNDR of the proposed ADC from input frequency range of 0.2MHz to 0.98MHz. The ENOB at Nyquist frequency is 7.56. This ENOB achieves Walden FOM [18] of 85fJ/conv. step. Fig. 13 shows the DNL and INL of the proposed ADC across 256 digital codes. The

worst case DNL is within 0.4LSB. INL is within 1LSB across all digital codes.

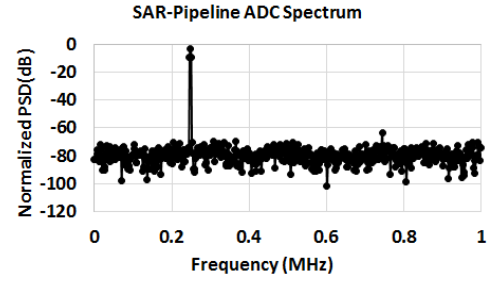


Fig. 9. Frequency spectrum of the proposed ADC ($F_{in}=248.34kHz$ & $F_s=2MHz$)

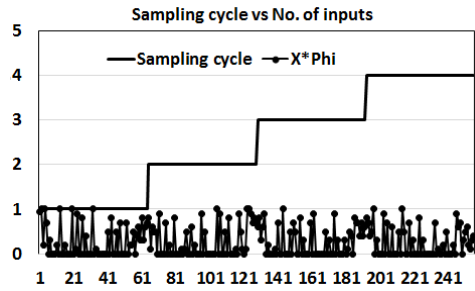


Fig. 10. 64 inputs for ADC for every 1 sampling cycle

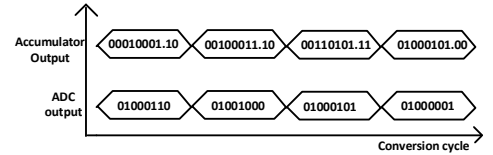


Fig. 11. Output of ADC and accumulator for 4 conversion cycle

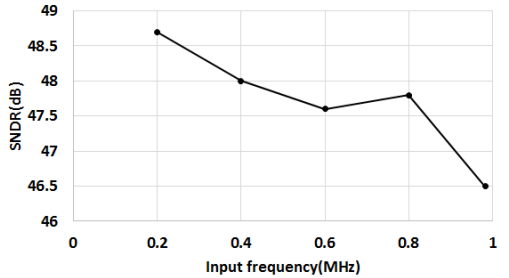


Fig. 12. Simulation result of SNDR vs Input frequency at $F_s=2MHz$

The power budget for the proposed ADC is given in Table .II. Even though the total power consumed from the supply is $50\mu W$, since the amplifier is shared between two ADC, the power for individual ADC's is $31\mu W$.

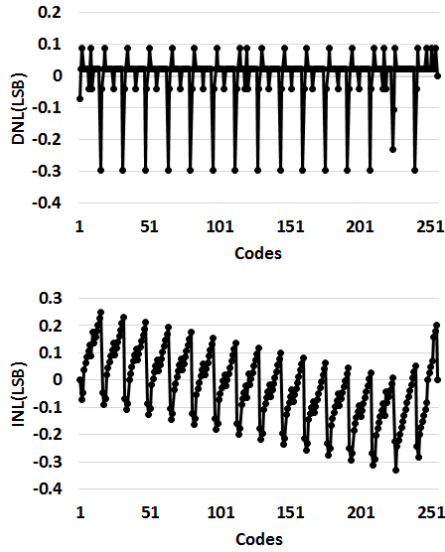


Fig. 13. DNL and INL of the proposed ADC across 256 codes

Block	Power/	Capacitance
SAR Stage1	$7\mu\text{W}$	28C
Amplifier	$41\mu\text{W}$	4C
SAR Stage1	$2.5\mu\text{W}$	10C
Accumulator	$0.5\mu\text{W}$	Nil

TABLE II. POWER AND CAPACITANCE CONTRIBUTION FROM INDIVIDUAL BLOCKS

Table. III shows the comparison of the proposed design with state of the art CS architecture. Proposed design is scalable and can handle a large number of inputs at the same time.

	Oike [5]	Guo [16]	Chen [10]	This work
ADC type	$\Sigma - \Delta$	SAR	SAR	SAR-Pipeline
Technology	$0.15\mu\text{m}$	$0.13\mu\text{m}$	$0.09\mu\text{m}$	$0.13\mu\text{m}$
Design	Measured	Simulated	Measured	Simulated
No. of inputs	1	4	1	64
Sampling cycles	256	1	256	4
F_s	NA	1MHz	2kHz	2MHz
Capacitance	NA	272C	256C	40C
Power	NA	$50\mu\text{W}$	$5\mu\text{W}$	$31\mu\text{W}$

TABLE III. COMPARISON WITH REPORTED WORKS

VII. CONCLUSION

A novel time interleaved sharing DAC is integrated with multiple column parallel SAR Pipeline ADC. The proposed architecture can be used for wearable devices with ultra-low power requirements. Our design and simulation results show 87fJ/conv. step with an average power of $31\mu\text{W}$.

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