All-Digital Low-Dropout Regulator With Adaptive Control and Reduced Dynamic Stability for Digital Load Circuits

Saad Bin Nasir, *Student Member, IEEE*, Samantak Gangopadhyay, *Student Member, IEEE*, and Arijit Raychowdhury, *Senior Member, IEEE*

***Abstract*—Digitally implementable LDOs embedded within digital functional units augment their analog counterparts for ultrafine-grained power management in digital ICs. Digital load circuits represent load currents with large and infrequent current transients and require a wide voltage range of operation, preferably down to the threshold voltage (V_{TH}) of the transistor. This paper presents a discrete-time, fully digital, scan-programmable LDO macro in a low-power 0.13-μm technology operating down to 1.07×, the transistor V_{TH}, and featuring greater than 90% current efficiency across a 50× current range through fine-grained clock gating and adaptive control. An 8× improvement in transient response time to large load steps is achieved through switched mode control. Both transient and steady-state operation models and measurements of the LDO are presented.**

***Index Terms*—Adaptive control, digital linear regulators, embedded power management, low power digital circuits.**

I. Introduction

DYNAMIC voltage and frequency scaling to manage power and performance of digital systems is a well-established technique. With the growing number of transistors per unit area, heterogeneity of load circuits, workload changes, thermal and process variations, the need for fine-grained temporal supply voltage management has become increasingly important. Similarly, many core systems and system-on-chip designs with multiple voltage domains further demand a spatially adjustable supply voltage network to enable chip scale energy optimality [1], [2]. With the growing number of such power states in any digital system, there is further demand on the voltage supply and regulation modules to not only provide an optimal spatio-temporal voltage management but also maintain high performance and energy efficiency across the entire current and voltage dynamic ranges. With all these power delivery constraints in perspective, a flexible and adaptive point of load (PoL) voltage distribution and regulation is needed. Analog PoL low dropout (LDO) regulators (typically targeted for sensitive analog load circuits) exhibiting high efficiency [3], fast small-signal response [4], [5], and high power supply rejection (PSR) [6] continue to be explored. However, with decreasing supply voltages, the bandwidth and performance of analog LDOs continue to decrease.

Recently, digital LDOs have been proposed which supplement their analog counterparts to realize an ultrafine grained spatio-temporal voltage distribution and regulation in digital ICs. Their compactness, ease of design, process scalability, and the opportunity to embed them deep within a digital functional unit make them suitable for PoL voltage regulation. Traditionally, analog LDOs have been employed for voltage sensitive analog load circuits which typically represent, mostly, dc loads. On the other hand, digital load circuits exhibit large load transients and wide operating voltages [from V_{MAX} to near-threshold voltages (NTV)]. Hence, linear regulators (including LDOs) that supply digital loads have a different value proposition, such as the capacity to operate at wide operating voltages and respond to large load steps. Further, they need to be synthesizable and process scalable. This is particularly true when the underlying load circuit is in a low-current/low-power state and needs to wake up in a few clock cycles. Other conventional metrics of analog LDOs, like voltage ripple, PSR can be relaxed, as these nonidealities add a small margin to the already existing voltage guard-band due to temperature, process, and aging. Recent demonstrations of all-digital LDOs [7]–[12] exhibit fully synthesizable and low-voltage designs and in a recent demonstration from Intel [10], a digital LDO has been used to power a graphics processor, further establishing the relevance and importance of all-digital LDO designs for wide-range digital load circuits.

Broadly, digital LDOs can be classified into continuous-time and discrete-time variants. Among the various continuous time digital LDOs, digital PID-based control mechanism used in [13], time to phase conversion implemented in [14], continuous asynchronous signaling used in [15], and a hybrid of analog and digital control sections demonstrated in [16] highlight recent progress. On the other hand, discrete-time implementations are fully synchronous. Bang-bang control-based designs used in [8], [9], and [11] are the typical examples of such a topology. In these discrete-time variants, output voltage is sampled with a master clock. Similarly, control signal generation and propagation is also synchronous. Furthermore, the designs presented in [8], [9], and [11] not only discretize the output stage but also operate power MOSFETs in triode; thus, eliminating any biasing requirements. Hence, following a discrete-time all-digital

Manuscript received August 25, 2015; revised November 12, 2015; accepted January 02, 2016. Date of publication January 19, 2016; date of current version July 08, 2016. This work was supported by the Semiconductor Research Corporation under task #1836.140 through the Texas Analog Center of Excellence, Intel and Qualcomm. Recommended for publication by Associate Editor K.-H. Chen.

The authors are with the Department of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332 USA (e-mail: saadbinnasir@gatech.edu; samantak8@gatech.edu; arijit.raychowdhury@ece.gatech.edu)

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2016.2519446

approach, a complete digital design can be achieved. It inherits the process and voltage scalability of digital logic and provides an opportunity to reuse power-gating transistors in a digital block as the output power MOSFETs.

In spite of their potential advantages in providing fine-grained voltage regulation, the baseline digital LDOs suffer from slower transient responses to large load current steps and show a trade-off between steady-state stability and transient response. This is due to their synchronous and sequential nature of switching. Further, the sampling frequency of the digital LDO (as discussed in Section II) controls its damping constant. Under a wide load range, the control loop can become power inefficient, heavily under-damped, and even unstable. We address these two critical challenges, namely; transient performance and loop stability in this paper, and propose an all-digital LDO with adaptive control for ultrawide dynamic range and reduced stability for fast large-signal transient response.

The LDO macrofabricated in a 0.13-μm LP CMOS technology features greater than 90% current efficiency across a 50$\times$ current range and 8$\times$ improvements in transient performance in response to large load current steps, which occur during wake up and clock gating/ungating among other large power state transitions of digital circuits. The baseline design comprises of a barrel shifter that digitally controls 128 identical output Power MOSFET (PMOS) transistors that provide regulation. To provide high efficiency with target stability under a large current range, we employ autonomous adaptation of the clock frequency F_S with changes in the load current. Similarly, to overcome the reduced gain offered by the output PMOS array working in triode region, we introduce reduced dynamic stability (RDS) through switched mode control as a design technique. The idea is to temporarily make the control loop marginally stable when a large load step has occurred. This makes the system more agile and faster in performance but does not compromise the run-time stability and enables high transient performance. The test-chip measurements corroborate with earlier modeling and analysis work by the authors and others, as we describe in this manuscript.

The rest of the sections are divided as follows. In Section II, the baseline design of the LDO macro is described with its linear transient control model and a nonlinear steady-state model. In Section III, implementation of the autonomous adaptation circuit is elaborated. It is followed by an introduction to the concept of RDS and its implementation in Section IV. Section V presents measurement results from a prototype test-chip and a comparison with competing designs. Finally, conclusions are drawn in Section VI.

II. Baseline Design

The baseline design of the all-digital LDO is presented in Fig. 1. The design consists of three major sections. The first section samples the output voltage and is implemented with a single-bit comparator. It is followed by a digital control section implemented through a barrel shifter. Finally, the output PMOS array provides load current and performs regulation [9].

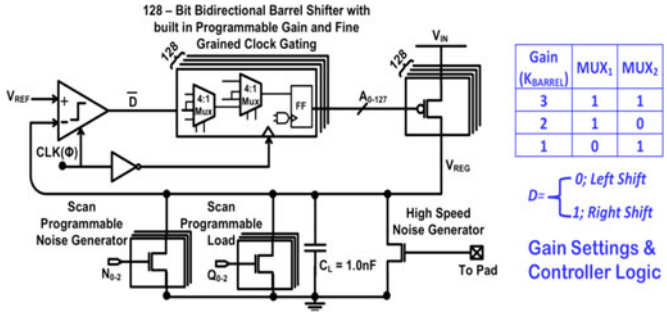


Fig. 1. Fully-digital low-dropout regulator with digitally programmable loop gain and fine-grained clock gating.

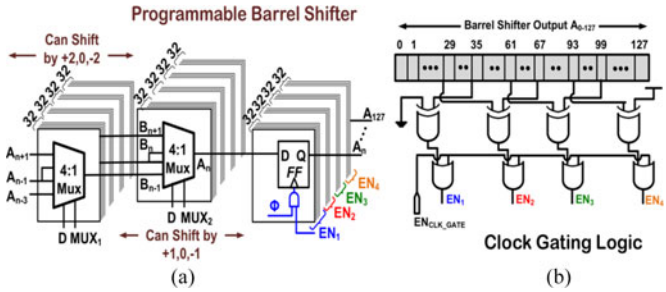


Fig. 2. (a) Externally programmable 128-bit barrel shifter with 32-bit sections clock gating. (b) Sliding clock gating signal generation.

A clocked sense amplifier-based comparator with an output latch [17] functions as a single-bit comparator. If output voltage $V_{\rm REG}$ is greater than $V_{\rm REF}$, the comparator outputs a "1" on the positive clock edge or a "0" otherwise. As compared to a clock-less op-amp-based comparator, this topology offers performance adaptation based on changing the clock frequency and reduces the static power consumption. The output from the comparator gives the shift direction to a 128-bit bidirectional barrel shifter. This barrel shifter has a modular design to allow both externally programmable gain and fine-grained clock gating. If $V_{\rm REG}$ is below $V_{\rm REF}$, more PMOS transistors are turned ON, translating into a right shift operation. Otherwise, a left shift is performed to turn OFF PMOS transistors. The barrel shifter is scan programmable and provides a shift of one, two, or three PMOS transistors in a single clock cycle. To reduce the propagation delay of the control signal, double clock edge triggering is employed. The comparator samples at the positive clock edge and the barrel shifter updates on the following negative clock edge. The magnitude of the shift in the barrel shifter serves as a gain control knob in the forward path of the LDO as we will explain later. The barrel shifter is implemented using two levels of signal multiplexing followed by a flip-flop. The first level of MUX allows a shift of $\{0, +2, -2\}$ and the second level of MUX gives $\{0, +1, -1\}$ to realize a complete shift range of $\{-3, -2, -1, 0, 1, 2, 3\}$. Here, "+" and "−" define right and left shifts, respectively. Register programmable control signals $\{\rm MUX_1, MUX_2\}$ are used to set the shift magnitude. This has been shown in Fig. 2(a).

Since the barrel shifter accounts for the largest digital part of the LDO and dominates the overall clock load, a fine-grained clock gating is implemented to enhance power efficiency of the overall system. The 128-bit barrel shifter is divided into four 32-bit sections, which are clock-gated in a sliding manner. Barrel shifter outputs are tapped from the boundary flip-flops of the 32-bit sections to generate enable signals for each 32-bit section, as shown in Fig. 2(b). For the maximum shift of three, clock gating enables the next section as soon as $((L \times 32) - 3)$th PMOS turns ON for an increasing load current. Here, L represents the enabled section and can be $\{1, 2, 3, 4\}$. Similarly, for a decreasing load current, a lower section is enabled as soon as $((L \times 32) + 3)$th PMOS turns OFF. This sliding logic keeps the relevant sections of the barrel shifter enabled while keeping the rest-clock gated. In the worst case, a maximum of two sections are enabled if the load conditions demand that PMOS transistors at the boundary of these two sections are ON.

The power output stage comprises of 128 PMOS transistors, which are operated in triode mode, thus, realizing a fully digital LDO implementation. The PMOS are equally sized with a width of 400 nm and a length of 120 nm each. The array can provide a maximum current of 4.6 mA for a dropout of 200 mV with $V_{\rm IN} = 1.0$ V. Scan programmable NMOS load transistors are implemented in the baseline design to achieve different values of steady-state load current. To analyze the transient performance of the LDO, another set of scan programmable but externally triggered NMOS transistors are used for creating large, programmable, and high-speed voltage droops. In the current design, a total capacitance of approximately ~900 pF is placed at the output node to mimic the capacitance offered by supply distribution grid (using metal routing) and a load digital functional unit [16]. In the next two sections, we present both a linearized model for transient analysis and a nonlinear model for limit cycle analysis in the digital LDO. These models have been presented in detail in [9] and [18] and are reported here briefly for the sake of completion and understanding trends in the measured data. Experimental results in Section V demonstrate the validity of these models.

A. Transient Behavioral Model

The presented LDO design is synchronous and its linear small signal model is represented in the z-domain. Following a similar analysis presented in [9], a second-order system dynamic model is shown in Fig. 3. An error sample is generated at every positive clock edge. In the control portion, after a half clock cycle delay, the barrel shifter produces a programmable shift with a gain $K_{\rm BARREL}$. Since this gain accumulates on the previous barrel shifter output, it acts as a perfect discrete-time integrator with a pole at $z = 1$. Since the barrel shifter output is held constant till the next negative clock edge, a zero-order hold is placed before the output stage. The output stage comprises of a power PMOS array and load circuit, which can be approximated as an *RC* load. This produces a first-order plant which exhibits a single pole at $Z = Z^{-F_{\rm LOAD}/F_S}$, where $F_{\rm LOAD}$ is the output pole frequency. The dc gain term in the load transfer function

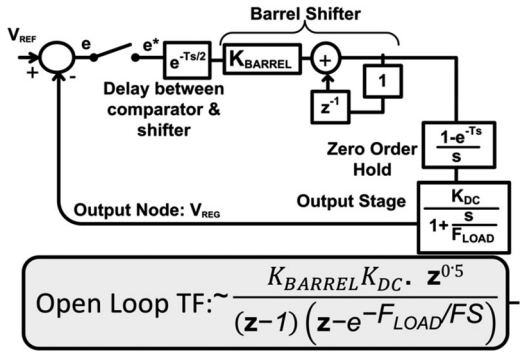


Fig. 3. Second-order discrete time transient model with open loop transfer function for the baseline design.

$K_{\rm DC}$ comes from the load current through the PMOS array. Using feedback theory, the open-loop transfer function between $V_{\rm REF}$ and $V_{\rm REG}$ can be written as

$$G(z) = \frac{K_{\rm FORWARD}\left(1 - e^{-F_{\rm LOAD}/F_S}\right)}{F_{\rm LOAD}} \times \frac{1}{(z-1)\left(z - e^{-F_{\rm LOAD}/F_S}\right)}. \quad (1)$$

Here, $F_{\rm LOAD} = 2\pi(R_{\rm LOAD}.C_{\rm LOAD})^{-1}$, $R_{\rm LOAD}$ can be approximated as $V_{\rm REG}/I_{\rm LOAD}$ and the total forward path gain is $K_{\rm FORWARD} = K_{\rm BARREL}K_{\rm DC}$. As evident from (1), one of the poles comes from the discrete integration at the unit circle boundary and the position of the other pole is given by both the load $F_{\rm LOAD}$ and the sampling F_S frequencies. A decreasing load current at iso-F_S decreases $F_{\rm LOAD}$ which brings the poles closer together on the real axis. In z-domain, this is equivalent to a decrease in the equivalent phase margin of the overall system. Therefore, the step response exhibits a higher overshoot and decreased damping resulting in an underdamped response. Similarly, an increase in the load current makes the whole system overdamped and shows greater stability but slower transient performance. This phenomenon is illustrated by the pole-zero plots and equivalent load-step response (simulation criteria reported in the figure caption) as shown in Fig. 4. On the other hand, increasing F_S enhances the transient performance of the whole system, but equivalently, the system becomes underdamped. For extremely light-load conditions, the system can become highly underdamped and eventually unstable. This motivates us to use an adaptive F_S, which can track $F_{\rm LOAD}$ during run-time such that the ratio $F_{\rm LOAD}/F_S$ is bounded and a target stability margin can be achieved across a wide dynamic range of load current conditions. The design details will be discussed in Section III. Further, faster rise-time and recovery from voltage droops of the output voltage can be achieved with an increased $K_{\rm BARREL}$, as illustrated from the simulation results in Fig. 5.

B. Steady-State Behavioral Modeling

The transient behavior model helps in understanding the LDO response to step changes in $V_{\rm REF}$ and $I_{\rm LOAD}$. This linear model

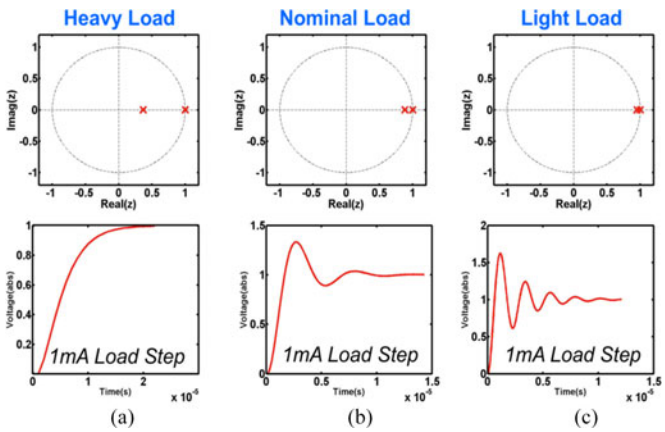


Fig. 4. Simulations showing a decrease in phase margin for a 1 mA load step with a constant $F_s = 50$ MHz for three different initial load conditions ($I_{\mathrm{Heavy\_load}} = 5$ mA, $I_{\mathrm{Nominal\_load}} = 1$ mA, $I_{\mathrm{Light\_load}} = 100$ mA).

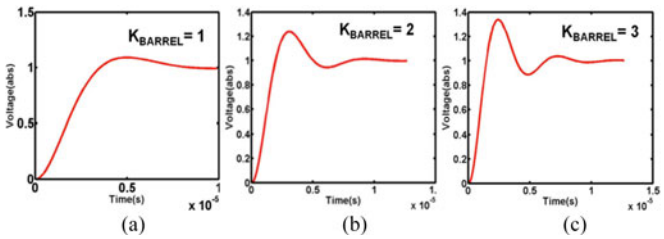


Fig. 5. A faster rise but increased overshoot is observed in simulations with increasing K_{BARREL}. Here the initial load is 1 mA, $F_s = 20$ MHz, and the load step is 500 mA.

is inadequate in understanding the steady-state behavior of a digital LDO which exhibits limit cycle oscillations [18]–[20]. For a constant I_{LOAD} and F_S, a voltage ripple is observed at the regulated output voltage. Since the PMOS transistors are operated as switches with a constant clock frequency, a number of these PMOS transistors turn "ON" and "OFF" periodically in steady state. The number of PMOS transistors turning "ON" and "OFF" periodically is referred to as the mode of oscillation (n). The Nyquist criterion is then applied to develop necessary conditions on the existence of different modes of limit cycle oscillation. Interested readers are pointed to [18] for more details on the model, and the key implications will be discussed here. As the sampling frequency F_S increases for iso-F_{LOAD} the mode of oscillation increases. One of the consequences of an increased mode of limit cycle oscillation is a potential increase in the output ripple. However, the ripple is not a direct function of n. As long as the mode of oscillation remains unchanged, a larger ratio F_S/F_{LOAD} tends to decrease the ripple due to the filtering action of the output pole. However, with increasing F_S/F_{LOAD}, the mode of oscillation itself increases discretely. This leads to discrete jumps in the ripple voltage as described in [18] and will be discussed in Section V.

C. Model Analysis

Based on the behavioral models for both transient and steady-state performance of the digital LDO, the following challenges of a baseline design can be ascertained.

1) Although a high F_S results in faster transient response but it renders the system underdamped. It exhibits loss of phase margin and results in large overshoot of the regulated voltage with slow settling. This leads us to the notion of keeping F_S/F_{LOAD} bounded for a more consistent transient response across a wide dynamic range of operation.
2) A high F_S/F_{LOAD} is responsible for a higher mode of limit cycle oscillation. However, as F_S/F_{LOAD} increases, the filtering action of the output pole tends to reduce the overall ripple. Conversely, at low F_S/F_{LOAD}, the output ripple due to the limit cycle becomes prominent.

Both of these factors dictate that F_S with respect to a given output pole F_{LOAD} needs to be bounded. This motivates the need for adaptation to enable wide dynamic range of operation. Simulations reveal that an F_S/F_{LOAD} ratio of five to ten provides an optimal tradeoff between response time and overshoot/phase-margin under constant load conditions [21].

III. Adaptation of Sampling Frequency With Changes in the Quiescent Point

In the current design, we perform an autonomous adaptation of F_S to ensure a consistent damping while maintaining a small ripple during steady state across the complete load range. As the load current is detected, it is used to select one of the three sampling clock frequencies $\{F_{\mathrm{HIGH}}, F_{\mathrm{NOM}}, F_{\mathrm{LOW}}\}$ once a steady state is established. These frequencies are generated through two current-starved voltage-controlled ring oscillators. VCO_1 provides F_{LOW} and F_{NOM} through its long and small chains, respectively, whereas VCO_2 provides F_{HIGH} and $F_{\mathrm{TRANSIENT}}$. $F_{\mathrm{TRANSIENT}}$ is used for large load transient events as explained later in Section IV. These VCOs provide tight frequency control with small power consumption and require no level shifting. The control voltages are accessible to the pads that allow us to calibrate F_S. The 128-bit output PMOS array is divided into three regions representing $I_{\mathrm{LIGHT}}, I_{\mathrm{NOM}}$, and I_{HEAVY} load conditions. I_{LIGHT} is classified until PMOS-45 turns ON. I_{NOM} extends to PMOS-85 from PMOS-45 and I_{HEAVY} starts from PMOS-85. The steady-state I_{LOAD} detector takes the control signals from the bit-45 and 85 of the barrel shifter. A change on any one of these control signals indicates a change of steady-state load region and creates a reset pulse for a 4-bit ripple carry adder. This adder is running from an external clock running at 5 MHz controlled through an I/O pad. The time of a 4-bit ripple carry adder to saturation serves as an incubation period for steady-state establishment, whereas a reset pulse before the adder saturates indicates a transient event. Once saturated, the adder stops and an appropriate F_S is selected to maintain a bounded F_S/F_{LOAD}. The F_S adaptation design is added to the baseline as illustrated in Fig. 6(a) with a representative timing diagram in Fig. 6(b). The inclusion of incubation period through the adder decouples the fast regulation loop from the slow F_S adaptation to keep the system stable. The classification of the load current into high, nominal, and low is based on a linear division of the total load range. It does not require any additional current detection hardware.

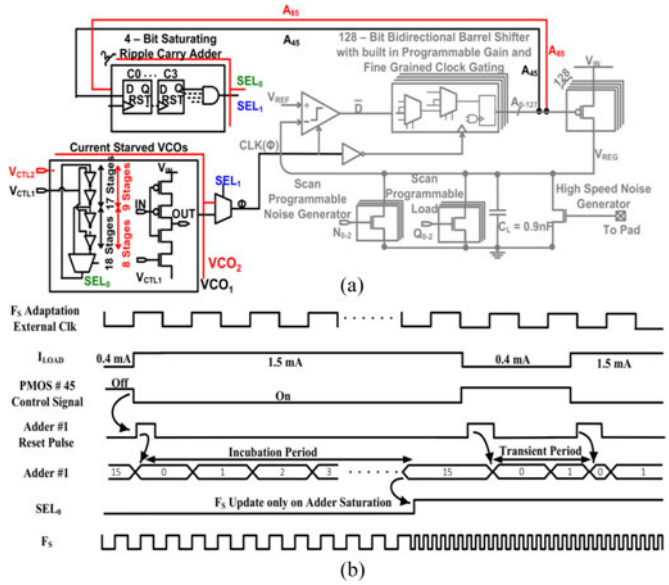


Fig. 6. (a) Autonomous adaptation of sampling frequency F_s across a wide dynamic range using current starved VCOs with steady state I_{LOAD} detection. (b) F_s adaptation timing diagram.

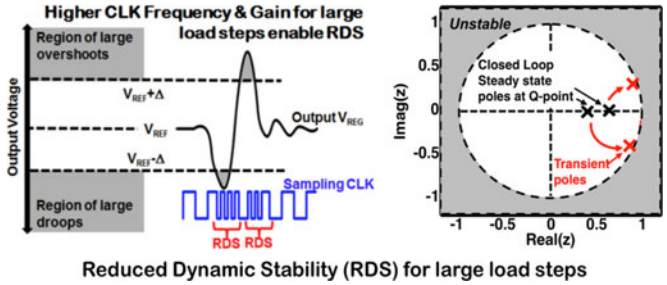


Fig. 7. Conceptual representation of temporary stability tradeoff for enhanced transient performance using RDS.

Without loss of generality, other nonlinear divisions are also possible.

IV. RDS-Based Fast Transient Control

A lower F_S saves controller power and maintains small signal stability. However, digital load circuits undergo very large and infrequent load transients (during power/clock gating/ungating). To address the limited run-time gain of the digital LDO, we introduce RDS as a solution to improve large signal transient response. RDS is based on the notion of switched mode control, where the control loop can discretely switch from a stable damped behavior to a quasi-stable behavior when the error voltage crosses a predetermined threshold Δ. The main objective of RDS is to create a system response which combines faster rise-time of an underdamped behavior and nonoscillatory settling of an overdamped behavior. To the author's knowledge, this is the first application of switched mode control in PoL linear regulation. Thus, for large voltage droops, the system switches to a fast F_S (underdamped) at a threshold $V_{\mathrm{REF}} - \Delta$ and comes back to slow F_S (overdamped) once V_{REG} is within some threshold Δ of V_{REF} as conceptually illustrated by Fig. 7.

A digital LDO allows a seamless implementation of RDS with minimal overhead of circuit complexity. Fast droop and overshoot detectors based on sense amplifier-based clocked comparators are placed in parallel with the basic comparator of the baseline design as shown in Fig. 8. V_{REG} is compared against a threshold Δ above and below V_{REF} and identifies an overshoot or droop. As soon as V_{REG} falls below $V_{\mathrm{REF}} - \Delta$, the droop detector selects a very fast sampling clock $F_{\mathrm{TRANSIENT}}$ available from VCO_2 ensuring a fast recovery. As soon as V_{REG} reaches back to $V_{\mathrm{REF}} - \Delta$, previously running steady state F_S clock is restored allowing a nonoscillatory return to the desired V_{REG}. Similarly, an overshoot is defined at a Δ above V_{REG}. In case of an overshoot due to a large load current decrease, $F_{\mathrm{TRANSIENT}}$ is enabled to ensure a fast return to the desired V_{REF}. A smooth monotonic return of the V_{REG} to V_{REF} is ensured by enabling the damped steady-state response of the LDO. This is done by switching over to the previously running steady-state F_S clock, once the V_{REG} reaches $V_{\mathrm{REF}} + \Delta$. Both upper and lower threshold voltages as well as the target reference voltage are externally available to the pads. This allows us to calibrate the threshold voltage Δ for different dropout voltages.

V. Test-Chip Measurement Results

The digital LDO is designed and fabricated in IBM 0.13-μm 8-M LP CMOS (process $V_{\mathrm{TH}} \approx 420$ mV at $V_{\mathrm{DS}} \approx 500$ mV) process. It occupies an active area of 0.355 mm^2 with both load capacitance and test load as shown in the chip micrograph of Fig. 9. The LDO is capable of regulating the output voltage from 1.1 to 0.45 V from a V_{IN} of 1.2 to 0.5 V with a minimum dropout of 50 mV as illustrated in the Shmoo plot of Fig. 10. The measured process V_{TH} is ~420 mV (at $V_{\mathrm{DS}} = 500$ mV), and thus, we can obtain regulation down to the NTV region ($V_{\mathrm{REG}} = 1.07$ of process V_{TH}). The LDO is measured to provide I_{LOAD} from 4.6 mA (maximum) down to 0.1 μA (minimum). Both externally controlled and scan programmable NMOS transistors are implemented as load. They are used to generate both fast transient step currents and quiescent currents, for complete characterization of slow adaptation and RDS across a wide dynamic range of load current. Fig. 11 illustrates the measured VCO frequency for the three steady-state VCO loops (high, nominal, and low) as a function of the control voltage V_{CONT}. As adaptive selection of F_S is employed, a representative oscilloscope capture Fig. 12 shows the autonomous change of F_S after an incubation time. Selection of F_S should ensure a target settling time for small load transients that happen during workloads on digital circuits in steady-state operation. Settling time T_S of load conditions from I_{LIGHT}, I_{NOM}, and I_{HEAVY} monotonically decreases for increasing F_S as the measurement results show in Fig. 13(a). For a target settling time, an adaptive F_S ensures consistent performance across the load current range. From Fig. 13(a) we note that for light load conditions, I_{LIGHT} meets an isosettling time constraint (of 1 μs) with a smaller F_S as compared to I_{NOM} and I_{HEAVY}. With increasing V_{REG}, a faster transient response is often desired. We calibrated V_{CONT} for three different settling time constraints $\{0.75, 0.65, 0.5\ \mu\mathrm{s}\}$ for V_{REG} between

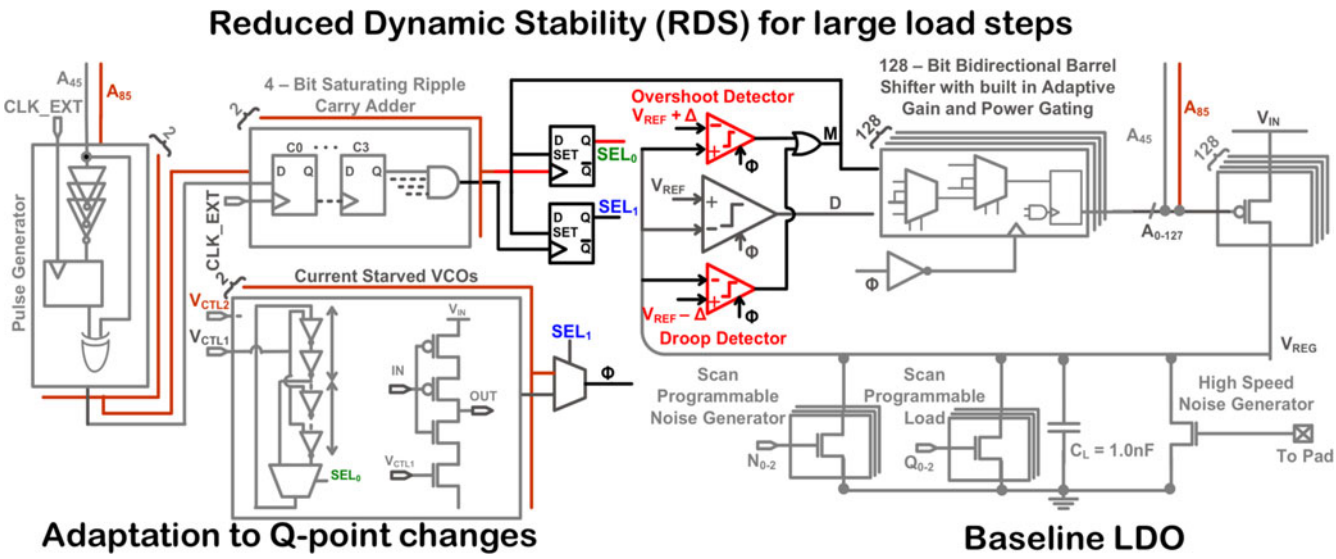
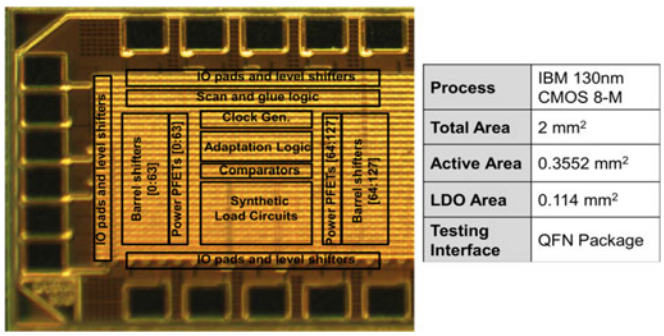


Fig. 8. Droop and overshoot detectors detect large load transients. In response, a faster sampling clock and higher loop gain are enabled for faster recovery from droops and overshoots.



Process	IBM 130nm CMOS 8-M
Total Area	2 mm^2
Active Area	0.3552 mm^2
LDO Area	0.114 mm^2
Testing Interface	QFN Package

Fig. 9. Chip micrograph, process and design specifications. The micrograph shows 1 mm $\times$ 1 mm which consists of the LDO and it shares the total 2 mm^2 area with another experiment.

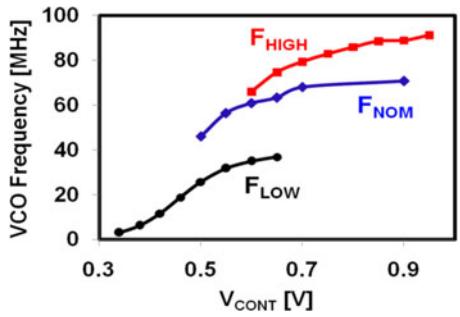


Fig. 11. Measured VCO frequency with varying $V_{\rm CONT}$. $V_{\rm CONT}$ is controlled and calibrated from an external pad.

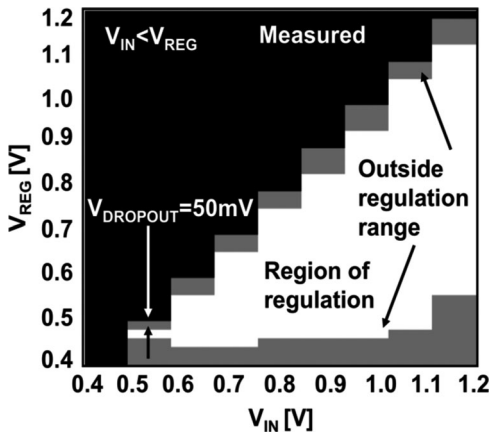


Fig. 10. Measured shmoo plot representing regulation range of the designed LDO. Transistor V_T is measured at 420 mV at $V_{\rm DS} = 500$ mV. The white region shows regulation, the gray region shows the region where regulation could not be obtained, and the black region shows an inoperable region where $V_{\rm IN} < V_{\rm OUT}$.

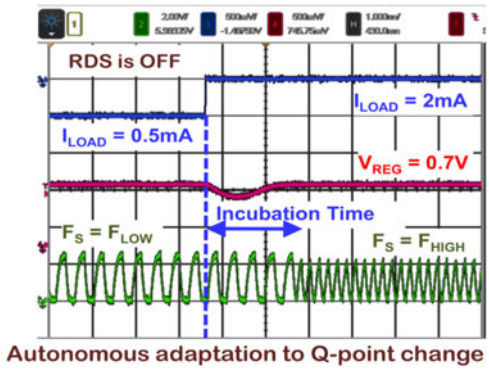


Fig. 12. Representative oscilloscope capture illustrating adaptation of F_s with change in the quiescent current.

0.5 and 0.8 V, and the corresponding frequencies are shown in fig. 13(b). These represent current loads that create voltage droops of 50 mV.

Large voltage droops associated with power state transitions shows a slow recovery in the baseline design motivating the use of RDS. A representative measured scope

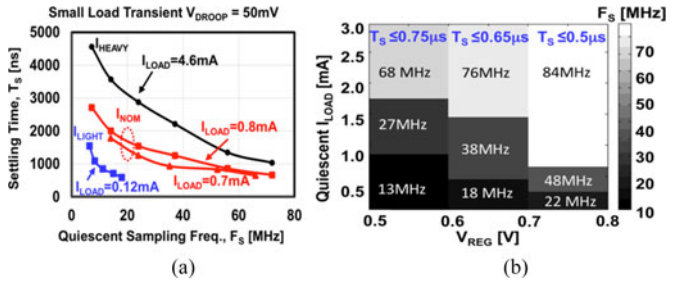


Fig. 13. (a) Measured settling time (T_s) for small voltage droops versus increasing F_s for multiple I_{LOAD} conditions. (b) Frequency selection plot for isosettling time performance for I_{LOAD} up to 3 mA using measurements. The different frequencies (as shown in the graph) are selected via calibration of on-die VCOs whose control terminal is exposed to the pads.

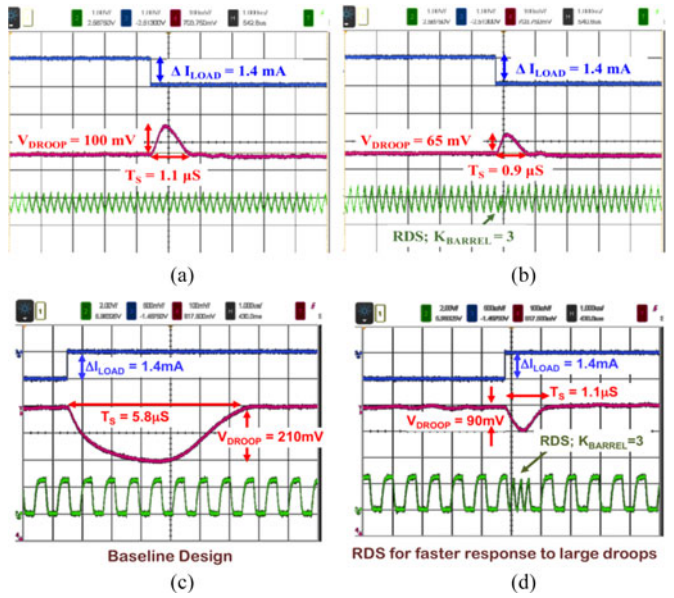


Fig. 14. Representative oscilloscope capture demonstrating RDS when a large voltage overshoot (droop) occurs in response to a large load step down (up) in (a) and (b) [(c) and (d)]. In digital circuits these are infrequent events that occur during clock/power ungating (gating).

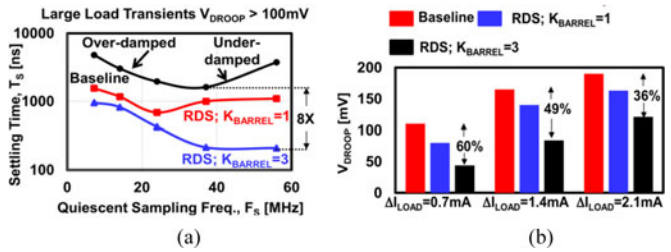


Fig. 15. Measured settling time, T_s (for small droops) with adaptation for autonomous choice of F_s. (a) RDS allows 8X improvement in TS for large load transients and (b) 36% to 60% reduction in V_{DROOP} when compared to the baseline design.

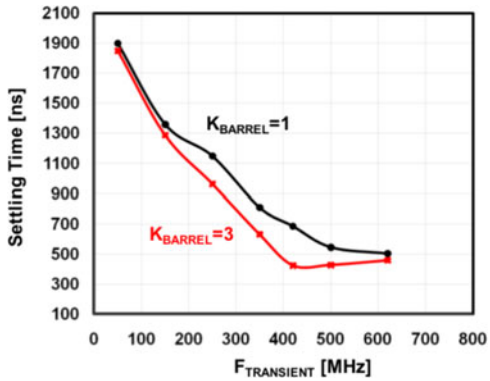


Fig. 16. Measured settling time with varying $F_{\mathrm{TRANSIENT}}$ for two different values of K_{BARREL}. Here, the initial load current is 1 mA, the lead step is 2 mA, and D = 25 mV. Optimal settling is achieved for an $F_{\mathrm{TRANSIENT}} \sim$ 425 MHz when steady state $F_s = 24$ MHz. We note that for high K_{BARREL} and $F_{\mathrm{TRANSIENT}} > 425$ MHz, the total system becomes underdamped and the settling time starts increasing.

capture is shown in Fig. 14, which shows switching to and from $F_{\mathrm{TRANSIENT}}$ resulting in a faster settling as well as reduced droop and overshoot compared to the baseline case ($\Delta = 50$ mV). During execution of a workload, the voltage transients on V_{REG} is expected to be less than 50 mV [10], and this sets the boundary between steady-state regulation and large signal transients. Measured settling time for droops >50 mV (in response to large current transients) is shown in Fig. 15. The settling time in the baseline design shows a concave behavior as seen in Fig. 15(a). Initially, increasing F_S decreases settling time as the system becomes critically damped but eventually becomes underdamped and exhibits large overshoot when F_S increases further. RDS helps reshape this concave settling behavior and reduce the settling time under large load steps (for a 2.1 mA load step). Along with switching to the transient frequency ($F_{\mathrm{TRANSIENT}} \sim 400$ MHz), the barrel shifter gain is also set to its highest scan programmable shift value (=3) to provide a high loop gain. Compared to the baseline design, an $8\times$ improvement in the settling time is measured. The greater agility achieved during the underdamped region of operation also helps in decreasing the overall voltage droop (for iso-load-step). A worst case of 36% and a best case of 60% reduction in droop is measured when RDS is used as compared to the baseline design [see Fig. 15(b)]. Fig. 16 illustrates the measured settling time with increasing $F_{\mathrm{TRANSIENT}}$ and constant F_S of 24 MHz. We note that the settling-time first decreases as $F_{\mathrm{TRANSIENT}}$ increases. However, as $F_{\mathrm{TRANSIENT}}$ increases beyond an optimal value, the composite system becomes underdamped and goes through larger and larger overshoots. This happens even when the sampling frequency is switched back once the output voltage reaches $V_{\mathrm{REF}} - \Delta$. This overshoot can be decreased by increasing Δ, which provides a tradeoff between performance and the region of operation when RDS is activated. For $\Delta =$ 50 mV and steady state $F_S = 24$ MHz, measurement results (see Fig. 16) show that $F_{\mathrm{TRANSIENT}}$ over 424 MHz exhibits underdamped response.

Fine-grained clock gating helps achieve large decrease in controller power. These power savings become higher as the operating frequency increases. Over 25% decrease in controller power is measured at a V_{IN} of 1 V and over 50% is achieved for 0.75 V at an F_S of 95 and 65 MHz, respectively, as shown in

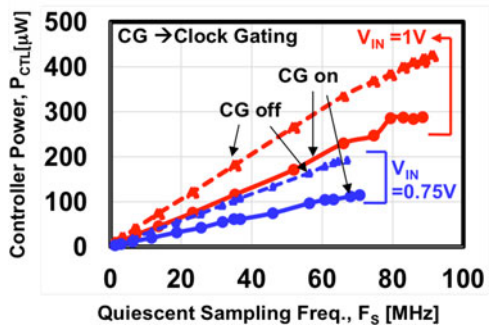


Fig. 17. Measured controller power reduction with clock gating.

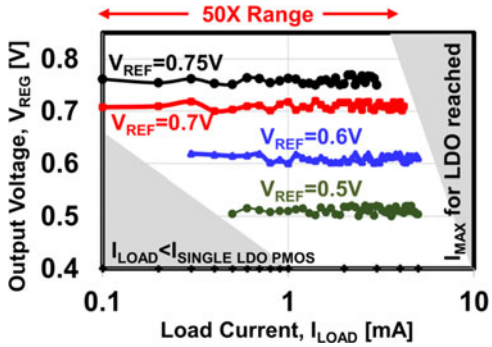


Fig. 18. Measured load regulation. The steady-state ripple of ∼10 mV limits the measurement of load regulation.

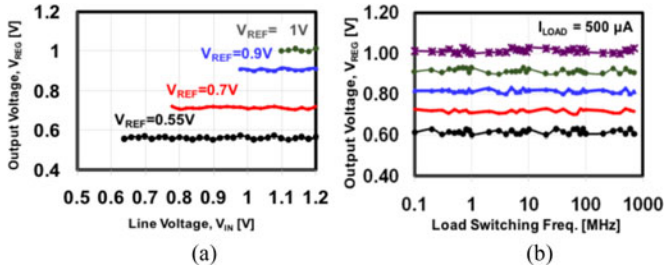


Fig. 19. (a) Measured line regulation for the LDO design. (b) Measured regulation against load switching frequency. The steady-state ripple of ∼10 mV limits the measurement of line-regulation and output voltage. The steady-state ripple forms a part of the V_{cc} guard-band.

Fig. 17. A 46× load current range from 0.1 μA (with a single PMOS turned ON) up to 4.6 mA is measured which shows regulation across the entire dynamic range. This is shown in Fig. 18, where the measured design regulates from 1.1 V down to 0.5 V with a minimum dropout of 50 mV. A measured load regulation (see Fig. 18) of <10 mV/mA is achieved. A worst-case line regulation of 3.4% is measured on $V_{\rm REG} = 0.55$ V for a $V_{\rm REG}$ of 0.55 to 1 V with $V_{\rm IN}$ ranging from 0.64 to 1.2 V as illustrated in Fig. 19(a). Similarly, a tight regulation of <5% (at worst-case) under a wide range of load switching frequency is measured as shown in Fig. 19(b). It should be noted that the measurement of load and line regulation are limited by the voltage ripple at the output, which is inherent in the design. This does not limit the usefulness of such digital LDOs in powering large digital

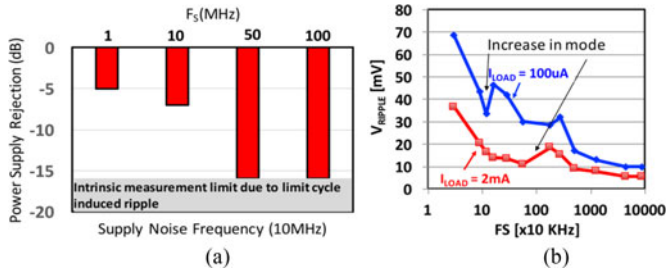


Fig. 20. (a) Measured supply rejection at 10 MHz of supply noise (with a supply ripple of 75 mV p-p) as a function of the sampling frequency and (b) Measured voltage ripple (maximum) measured for a wide range of F_S. We note that for low F_S, an increase in F_S causes increase in the mode of oscillation that leads to sudden jumps in the ripple voltage. As F_S increases, the output pole filters out the ripple noise and a residual ripple voltage of 10 mV is noted at $F_S \sim 100$ MHz.

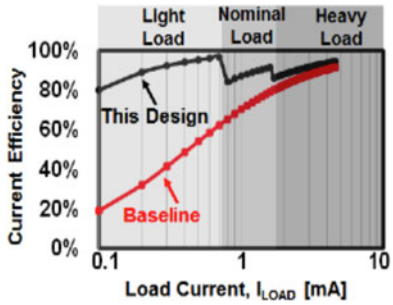


Fig. 21. Measured current efficiency across the complete load range.

circuits, as has been demonstrated in [10]. The supply rejection at 100 MHz of supply ripple (with p-p ripple of 75 mV) shows that an increasing F_S leads to higher loop gain and better supply rejection with a maximum measured rejection of −16 dB. This is shown in Fig. 20(a). We also measure the maximum voltage ripple during steady-state as a function of F_S [see Fig. 20(b)]. For low F_S, the ripple is large and we note discrete jumps as the system switches to a higher mode of limit cycle oscillation. This corroborates the theory that is discussed in Section II-B and [18]. With increasing F_S, the output pole tends to filter out the voltage ripple and an inherent ripple of ∼10 mV is measured at $F_S = 100$ MHz. Controller current measured through an ammeter connected between an external power supply and controller supply pins shows a 4× improvement in current efficiency at light load conditions through adaptation when compared to the baseline design (see Fig. 21). A comparative study with recently published data establishes that the current design (see Table I) is competitive in both power efficiency and performance. A power efficiency figure of merit (FOM1), defined as the average current efficiency across a load range from $I_{\rm MAX}$ to $I_{\rm MIN}$ is >90%, compared to <56% for previously published data, where no load current-based adaptation has been shown. RDS, which enables a dynamic tradeoff between instantaneous stability and transient response, provides an ultrafast transient response with a discrete-time digital loop, without compromising the run-time stability. FOM2 [4], normalized to the process node in a manner done in [22], shows that the performance is comparable to its analog counterparts.

TABLE I
COMPARISON WITH PUBLISHED LDO DESIGNS

	This Work	[14]	[8]	[15]
Type	LDO	LDO	LDO	LDO
Technology	130 nm	65 nm	40 nm	45 nm SOI
Control methodology	digital	digital	digital	multiloop Analog
Adaptive Control	Yes	No	No	No
RDS	Yes	No	No	No
V_{in} (V)	0.5–1.2	0.6	0.5	1.179–1.625
V_{out} (V)	0.45–1.14	0.4	0.45	0.9–1.1
Load Current : l_{max} (mA)	4.6	200	0.2	42
Load Regulation (mV/mA)	<10 mV/V*	0.05	0.65	9.8
Line Regulation or PSR	-16 dB at 10 MHz	-13 dB	3.1 mV/V	NA
Controller Current : l_{CTL} (uA)	$\sim$751	25.1	2.7	9450
Active Area (mm^2)	0.114	0.0375	0.042	0.075
Peak Current Efficiency [%]	98.30	99.99	98.70	77.50
Max voltage droop at Load Step	<40 mV at 0.7 mA	NA	40 mV at 200 μA	$\sim$7.6 at 4.5 mA
FOM1 [%]	90.80%	NA	55.40%	44.90%
FOM2 (process normalized) [ns]	0.036	NA	270	0.0624

FOM1—Efficiency Metric–Average current efficiency across a 50X current dynamic range.
FOM2—Performance Metric–(Transient Time)* l_{CTL}/l_{max}.
*Load regulation is below the intrinsic ripple limit of ~ 10 mV/V which is inherent because of the limit cycle oscillations.
NA—Insufficient data.

VI. CONCLUSION

This paper presents a discrete time all-digital LDO which can be embedded in digital designs for fine-grained power management. A current efficiency over 90% across the load current range is measured with an $8\times$ improvement in transient response time to large load steps. The concepts of adaptive control and RDS for performance enhancements are shown. Measurements are performed on a 0.13-μm test-chip which shows competitive FOM with the current state-of-the-art LDO designs which are targeted for digital load circuits.

REFERENCES

[1] C. Tokunaga, J. F. Ryan, C. Augustine, J. P. Kulkarni, Y-C. Shih, S. T. Kim, R. Jain, K. Bowman, A. Raychowdhury, M. M. Khellah, J. W. Tschanz, and V. De, "5.7 A graphics execution core in 22 nm CMOS featuring adaptive clocking, selective boosting, and state-retentive sleep," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2014. pp. 108–109.

[2] H. Mair *et al.*, "23.3 A highly integrated smartphone SoC featuring a 2.5 GHz octa-core CPU with advanced high-performance and low-power techniques," presented at the IEEE International Solid-State Circuits Conf. Digest Technical Papers, San Francisco, CA, USA, Feb. 2015.

[3] G. A. Rincón-Mora and P.E. Allen, "A Low-voltage, low quiescent current, low drop-out regulator," *IEEE J. Solid-State Circuits*, vol. 33, no. 1, pp. 36–44, Jan. 1998.

[4] P. Hazucha, T. Karnik, B. A. Bloechel, C. Parsons, D. Finan, and S. Borkar, "Area-efficient linear regulator with ultra-fast load regulation," *IEEE J. Solid-State Circuits*, vol. 40, no. 4, pp. 933–940, Apr. 2005.

[5] Y. H. Lam and W. H. Ki, "A 0.9V 0.35 μm adaptively biased CMOS LDO regulator with fast transient response," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, pp. 442–626, Feb. 2008.

[6] M. El-Nozahi, A. Amer, J. Torres, K. Entesari, and E. Sánchez-Sinencio, "High PSR low dropout regulator with feed-forward ripple cancellation technique," *IEEE J. Solid-State Circuits*, vol. 45, no. 3, pp. 565–577, Mar. 2010.

[7] J. J. Chen, M.-S. Lin, H.-C. Lin, and Y.-S. Hwang, "Sub-1V capacitor-free low-power-consumption LDO with digital controlled loop." In *Proc. IEEE Asia-Pac. Conf. Circuits Syst.*, pp. 526–529, Nov./Dec. 2008.

[8] Y. Okuma, K. Ishida, Y. Ryu, X. Zhang, P.-H. Chen, K. Watanabe, M. Takamiya, and T. Sakurai, "0.5-V input digital LDO with 98.7% current efficiency and 2.7-uA quiescent current in 65 nm CMOS," presented at the IEEE Custom Integration Circuits Conf., San Jose, CA, USA, Sep. 2010.

[9] S. Gangopadhyay, Y. Lee, S. B. Nasir, and A. Raychowdhury, "Modeling and analysis of digital linear dropout regulators with adaptive control for high efficiency under wide dynamic range digital loads," presented at the Design Automation Test Europe Conf., Dresden, Germany, Mar. 2014.

[10] S. T. Kim, Y.-C. Shih, K. Mazumdar, R. Jain, J. F. Ryan, C. Tokunaga, C. Augustine *et al.*, "Enabling wide autonomous DVFS in a 22 nm graphics execution core using a digitally controlled hybrid LDO/switched-capacitor VR with fast droop mitigation," presented at the IEEE Int. Solid-State Circuits Conf. Digest Technical Papers, San Francisco, CA, USA, Feb. 2015.

[11] S. B. Nazir, S. Gangopadhyay, and A. Raychowdhury, "5.6 A 0.13μm fully digital low-dropout regulator with adaptive control and reduced dynamic stability for ultra-wide dynamic range," presented at the IEEE Int. Solid-State Circuits Conf. Digest Technical Papers, San Francisco, CA, USA, Feb. 2015, pp. 1–3.

[12] Y. Fan and P. K. T. Mok, "Fast-transient asynchronous digital LDO with load regulation enhancement by soft multi-step switching and adaptive timing techniques in 65-nm CMOS," presented at the IEEE Custom Integrated Circuits Conf., San Jose, CA, USA, Sep.2015.

[13] K. Otsuga, M. Onouchi, Y. Igarashi, T. Ikeya, S. Morita, K. Ishibashi, and K. Yanagisawa, "An on-chip 250 mA 40 nm CMOS digital LDO using dynamic sampling clock frequency scaling with offset-free TDC-based voltage sensor," in *Proc. IEEE Int. SOC Conf.*, Sep. 2012, pp. 11–14.

[14] S. Gangopadhyay, D. Somasekhar, J. W. Tchanz, and A. Raychowdhury, "A 32 nm embedded, fully-digital, phase-locked low dropout regulator for fine grained power management in digital circuits," *IEEE J. Solid-State Circuits*, vol. 49, no. 11, pp. 2684–2693, Nov. 2014.

[15] C.-C. Chiu, P.-H. Huang, M. Lin, K.-H. Chen, Y.-H. Lin, T.-Y. Tsai, C.-C. Huang, and C.-C. Lee, "A 0.6 V resistance-locked loop embedded digital low dropout regulator in 40 nm CMOS with 77% power supply rejection improvement." in *Proc. Symp. VLSI Circuits*, Jun. 2013, pp. C166–C167.

[16] J. F. Bulzacchelli *et al.*, "Dual-loop system of distributed microregulators with high DC accuracy, load response time below 500 ps, and 85-mV dropout voltage," *IEEE J. Solid-State Circuits*, vol. 47, no. 4, pp. 863–874, Apr. 2012.

[17] B. Nikolic, V. G. Oklobdzija, V. Stojanovic, W. Jia, J. K.-S. Chiu, and M. M.-T. Leung, "Improved sense-amplifier-based flip-flop: Design and measurements," *IEEE J. Solid-State Circuits*, vol. 35, no. 6, pp. 876–884, Jun. 2000.

[18] S. B. Nasir and A. Raychowdhury, "On limit cycle oscillations in discrete-time digital linear regulators," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2015, pp. 371–376.

[19] S. R. Sanders, "On limit cycles and the describing function method in periodically switched circuits," *IEEE Trans. Circuits Syst. I*, vol. 40, no. 9, pp. 564–572, Sep. 1993.

[20] V. Velde and E. Wallace, *Multiple-Input Describing Functions and Nonlinear System Design*. New York, NY, USA: McGraw-Hill, 1968.

[21] S. B. Nasir and A. Raychowdhury. (2015, Jan.). "A model study of an All-digital, discrete-time and embedded linear regulator," arXiv 1501.00579 [cs.AR], [Online]. Available: http://arxiv.org/abs/1501.00579.

[22] A. Raychowdhury, C. Tokunaga, W. Beltman, M. Deisher, J. Tschanz, and V. De, "A 2.3nJ/Frame voice activity detector for context-aware systems in 32 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 48, no. 8, pp. 1963–1969, Aug. 2013.

Saad Bin Nasir (S'13) received the B.S. degree in electrical engineering from the National University of Sciences and Technology, Islamabad, Pakistan, in 2010, and the M.S. degree from the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA, USA, in 2014, where he is currently working toward the Ph.D. degree.

His industry experience includes three years as a Design Engineer at Center for Advanced Research in Engineering, Islamabad. His research interests include integrated circuit design and applied control theory with a current focus on modeling, design and development of adaptive power management in nanoscale integrated circuits.

Samantak Gangopadhyay (S'13) received the B.Tech. and M.Tech. degrees in electronics and electrical communication engineering with a specialization in microelectronics and VLSI design from the Indian Institute of Technology, Kharagpur, West Bengal, India, in May, 2009.

After graduation, he joined the IBM India as a Physical Design R&D Engineer to work on the power series and Z-mainframe microprocessors. In this role, he was responsible for the implementation of synthesizable circuits while satisfying timing, power, noise, electromigration, design-for-test, and design-for-manufacturing specifications. In 2013, he started his Doctoral Program at the Georgia Institute of Technology, Atlanta, GA, USA, while joining the Integrated Circuits and Systems Research Laboratory. His research interests include the design of low power digital circuits, low-dropout voltage regulators, and power management for wide dynamic range computation.

Arijit Raychowdhury (M'07–SM'13) received the B.E. degree in electrical and telecommunication engineering from Jadavpur University, Kolkata, India, and the Ph.D. degree in electrical and computer engineering from Purdue University, West Lafayette, IN, USA.

He is currently an Associate Professor at the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA, USA, where he currently holds the Semiconductor Junior Research Professorship. He joined Georgia Tech in January 2013. His industry experience includes five years as a Staff Scientist in the Circuits Research Lab, Intel Corporation and a year as an Analog Circuit Designer with Texas Instruments Inc. His research interests include digital and mixed-signal circuit design, design of on-chip sensors, memory, and device-circuit interactions.

Dr. Raychowdhury holds more than 25 U.S. and international patents and has published more than 100 articles in journals and refereed conferences. He received the Intel Early Career Faculty Award in 2015; the NSF CRII Award in 2015; the Intel Labs Technical Contribution Award in 2011; the Dimitris N. Chorafas Award for outstanding doctoral research in 2007; the Best Thesis Award, College of Engineering, Purdue University in 2007; the Best Paper Awards at the International Symposium on Low Power Electronic Design in 2006 and 2012; IEEE Nanotechnology Conference in 2003; the SRC Technical Excellence Award in 2005; Intel Foundation Fellowship in 2006, NASA INAC Fellowship in 2004, and the Meissner Fellowship in 2002.