Analysis of Defects and Variations in Embedded Spin Transfer Torque (STT) MRAM Arrays

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***Abstract*—Spin transfer torque magnetic random access memory (STT-MRAM) is a competitive, future memory technology for last-level embedded caches. It exhibits ultra-high density (3–4X of SRAM), non-volatility, nano-second Read and Write speeds, and process and voltage compatibility with CMOS. As the design and fabrication process mature for the STT-MRAM, there is a need to study the various fault models that can affect this novel memory technology. This work presents a comprehensive analysis of fault models which represent both parametric variations as well as defects (opens and shorts) in STT MRAM. Sensitivity of Read, Write and Retention to process (material and lithographic) parameters, defects (both intra-cell and inter-cell) and data patterns are studied.**

***Index Terms*—Defects, spin transfer torque magnetic random access memory (STT-MRAM), testing, variations.**

I. Introduction

With an ever-increasing demand for larger on-die memory and traditional CMOS scaling hitting the atomic scale boundaries [1], there is an urgent need to explore novel memory technologies. Many CMOS hybrid memory technologies like STT-MRAM, R-RAM, PCM, are being considered by the research community and industry today to replace the traditional SRAM based on-die memory. These memories use nanoscaled devices with unique material properties that change state under the influence of electric or magnetic fields. These state changes are leveraged for bit level storage. Since such state changes are preserved even after removing the stimulus and supply, these CMOS hybrid technologies offer high levels of non-volatility. Among these, Spin Torque Transfer (STT)-MRAM is considered a promising candidate as an alternative to embedded DRAM (eDRAM) and SRAM due to its high density, non-volatility, high endurance, easy integration with the existing CMOS fabrication process and nanosecond access times [1]–[3]. It has emerged as a successor to MRAM by providing current induced write in scaled process nodes [1]. The huge potential of STT-MRAM as a viable embedded memory technology at advanced process nodes has been well demonstrated in the 45 nm [4] and 65 nm [5] technology nodes. As the STT-MRAM technology continues to mature, rigorous analysis of variability and failure in this novel resistive memory need to be studied in detail. Previous research [6]–[10] has reported the effects of parametric variations in the read and write access times and failure probabilities in STT-MRAM. On the other hand, the effects of defects and the corresponding failure models in STT-RAM have not been extensively studied. The defect and fault models of SRAM have been studied in past research such as [11]–[13]. More recently, research [14]–[18] has addressed fault modelling in Memristor arrays by injecting electrical defects and identified possible faults in Memristor arrays. But, because of the fundamental differences in operation between SRAM, Memristor and STT-MRAM, not all fault types discussed in previous research is applicable to STT-MRAM. As an example, STT-MRAM, being a truly bi-stable device, does not suffer from the dynamic Write disturb Fault (dWdF) identified in [17]. Also, [14], [17] mostly identify static fault models due to the injected electrical faults. However, there are also many dynamic faults that are possible due to simultaneous switching of two cells together in presence of bridge defects. In addition, STT-MRAM faces its own unique set of possibilities of failure and faults due to parametric variations and injected defects, which we explore in this paper.

To the best of authors' knowledge, this is the first research that systematically explores and analyses all possible defects and fault models in STT-MRAM arrays. In this work, we aim to provide a comprehensive treatment and classification of the fault models manifesting due to both parametric variations and electrical faults in STT-MRAM memory arrays. We consider the three main modes of failure—Read failure, Write failure and Retention failure that are prevalent in STT-MRAM and analyze the fault models that lead to these failures.

- We study sensitivity of Write (WR) and Read (RD) with the parameter variations and identify the fault models that manifest due to variations. Failure probability of Write, Read and Retention are studied.
- We inject electrical faults at an array level and formulate the fault primitives occurring in the cell, thus documenting the discovered Data-dependent Coupling Faults. Further, we identify the data patterns that sensitize each of the documented faults leading to failure.
- We consider the interplay of parameter variations and electrical faults and effect on failure.

Manuscript received July 08, 2015; revised September 04, 2015; accepted October 12, 2015. Date of publication April 20, 2016; date of current version September 09, 2016. The work of Ashwin Chintaluri was supported by the Semiconductor Research Corporation (TASK 2493.001). This paper was recommended by Guest Editor X. Li.

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Digital Object Identifier 10.1109/JETCAS.2016.2547779

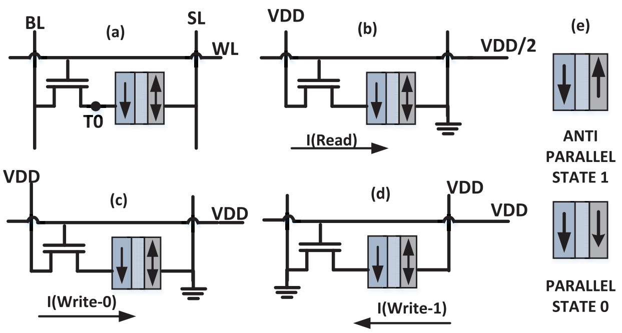


Fig. 1. (a) Basic 1T-1MTJ cell. (b) Bias condition for read. (c) Write 0 bias condition. (d) Write 1 bias condition. (e) States in a MTJ due to orientation of magnetic moments.

This paper is divided as follows. In Section II, we describe the operation of STT-MRAM bit cells and in Section III an end-to-end and vertically integrated model capable of simulating STT-MRAM from devices to arrays is described. Section IV describes the role of parametric variations in fault models. In Section V, possible defects (resistive opens and shorts) within a cell (intra-cell) and cell-to-cell (inter-cell) are shown and their effects are discussed. Section VI discusses the test patterns needed to sensitize the faults and finally conclusions are drawn in Section VII.

II. The Basic 1T-1R STT-MRAM Cell

When a spin-polarized current passes through a mono-domain ferromagnet, it attempts to polarize the current in its preferred direction of magnetic moment. As the ferromagnet absorbs some of the angular momentum of the electrons, it creates a torque that causes a flip in the direction of magnetization in the ferromagnet. The basic STT-MRAM cell comprises of an access transistor and a Magnetic Tunneling Junction (MTJ) as shown in Fig. 1(a). The MTJ, which is the storage element in the cell, consists of a tunneling oxide (MgO) sandwiched between two ferromagnetic layers (CoFeB based), one of which has a fixed magnetization and the other is a free layer. The fixed layer is the polarizer (reference) and the free layer acts as the storage node. The relative alignment of the ferromagnetic layers results in a high resistance path (anti-parallel) or a low resistance (parallel) path for the current, giving a notion of binary storage. Depending on the direction of current of a sufficient density, the free layer magnetization flips from Anti-parallel to Parallel state or vice versa resulting in change of bit from 1 to 0 or 0 to 1, respectively. Fig. 1(b)–(d) illustrates the bias conditions applied for the read and write operations. For our study, we consider that the fixed layer is connected to the access transistor. As one can see, the write operation is bidirectional, where either the bit-line (BL) or source line (SL) is pulled high and the other one is pulled low depending on the polarity of the write operation. The read operation is unidirectional with an under-driven word line voltage (WL), where a pre-charged BL voltage is allowed to discharge through the cell, the rate of discharge governed by the resistive state of the cell.

For an STT-MRAM cell to qualify as a non-volatile memory cell, it should satisfy the fundamental properties of readability, writability and stability (retention) [19]. These three properties depend closely on the material, electrical and design parameters of both the MTJ as well as the access transistor. The key macroscopic parameters whose variations control the overall failure probabilities in STT-RAM arrays are as follows.

1) **MTJ Material parameters:**
   a) The magnetic anisotropy $(\mathrm{H_K})$.
   b) Saturation magnetization $(\mathrm{M_S})$.
   c) Tunnel Magneto-resistance ratio (TMR).
   d) Oxide thickness of MgO layer $(\mathrm{T_{OX}})$.
2) **Transistor Electrical parameters:**
   a) Threshold voltage $\mathrm{V_{TH}}$ of the access transistor.
3) **Design Parameters (Lithographic):**
   a) Planar dimensions of the MTJ and Length and Width variations of the access transistor.

In addition, the thermal stability factor for an STT-MRAM, which is defined by a measure of the stored internal energy, is estimated as $\Delta \sim 1/2\mathrm{M_S H_K V}$, where V is the total volume of the free layer nanomagnet. Authors in [2], [6], [8], [20], [21] explore the design space for some of these parameters with an emphasis on scalability. To understand the role of the design and material parameters in the process of read and write, a complete solution of the magnetic dynamics under a spin transfer torque current needs to be analyzed. This is typically done using a macrospin approximation of the free layer nanomagnet, as has been proposed in [22]. A solution of the linearized Landau-Lifshitz-Gilbert (LLG) equation with the spin torque current demonstrates the close interaction of the device magnetics and the injected current. The linearized LLG equation is numerically solved to understand the switching dynamics of the free-layer magnetic-moment $\boldsymbol{m}(\boldsymbol{t})$ in presence of the torque experienced because of uniaxial anisotropy field $(\mathbf{T_U})$, easy plane anisotropy field $(\mathbf{T_K})$, and spin transfer torque from injected electrons $(\mathbf{T_S})$. The LLG under the total torque $(\mathbf{T})$ is expressed as

$$\frac{d\boldsymbol{m}(t)}{dt} + \left(\boldsymbol{m}(t) X \frac{d\boldsymbol{m}(t)}{dt}\right) = \gamma \boldsymbol{T} \tag{1}$$

where α is the LLG damping coefficient γ is the gyromagnetic ratio. The solution of (1) is carried out in polar coordinates, and the transformed equation is

$$\frac{1+\alpha^2}{\gamma H_K}\begin{bmatrix}\frac{d\theta}{dt}\\ \frac{d\phi}{dt}\end{bmatrix} = \boldsymbol{T_U} + \boldsymbol{T_K} + \boldsymbol{T_S} \tag{2}$$

where the free layer nanomagnet is in the $\phi = \pi/2$ plane. In a manner described in [17], the switching current density $(\mathrm{J_{C0}})$ at $\mathrm{T} = 0\mathrm{K}$ can be described by

$$J_{C0} = \left(\frac{2e}{\hbar}\right)\left(\frac{\alpha}{\eta}\right)(tM_S)(H_K + 2\pi M_S) \tag{3}$$

where e is the electronic charge, η is the polarization of the injected current, and t is the thickness of the free layer.

At non-zero temperatures, the thermal activation factor assists in switching and is included using a stochastic thermal model as described in [6]. More details of the model and its integration in the array level simulator are described in Section III. Equations (1)–(3) describe the process of write in STT-MRAM.

The process of read is based on an electrical read-out of the difference in resistance between the parallel and anti-parallel configurations of the MTJ stack. A key material and design parameter, the Tunnel Magneto-resistance Ratio (TMR) is the ratio of difference between the high resistance, $\mathrm{R_H}$ (anti-parallel state) and low resistance $\mathrm{R_L}$ (parallel state) to the resistance $\mathrm{R_L}$ and is given by

$$TMR = \left(\frac{R_H - R_L}{R_L}\right) \cdot 100\%. \quad (4)$$

A high TMR assists in a stable, error free read even under process induced variations. In the following sections, we explore the effects of process induced variations and defects on the process of read, write and retention.

III. Model and Simulation Infrastructure Development

The simulation model is based on the macrospin assumption of the free-layer nanomagnet [6], [22] as described in Section II. In our current study, an HSPICE based model for STT-MRAM has been developed using controlled current and voltage sources that emulate the spin dynamics. Details of the model development have been extensively reported in [6], [10], [23] and will not be discussed here. Interested readers are pointed to [23] for numerical techniques to solve LLG with spin transfer torque and to [10] for details on HSPICE compatible STT-MRAM models. The resistance of the MTJ stack, as the magnet undergoes precession from $\theta = 0$ to $\theta = \pi$ to is given by

$$R(\theta, V, T) = \frac{\sin(cT)}{cT}[P_3\theta^3 + P_2\theta^2 + P_1\theta + R_L] \left(1 - \frac{abs(V)}{Slope}\right) \cdot 10^{s(T_{OX} - T_{OX,0})} \quad (5)$$

where, V is applied voltage, c is a material constant, P_{1-3} are fitting parameters and $Slope$ determines voltage dependence of R_H. This also captures the temperature dependence of resistance with the operating temperature (T). The MTJ model is fully parameterized using device and material parameters discussed in the next section, which allows comprehensive variation analysis. Variation analysis is done through extensive Monte Carlo simulations where both device-to-device and temporal variations are accounted for. This device model is incorporated in a bit-cell with a 2-fin FinFET selector transistor from a 14 nm process node [24] and the design has been scaled up to an array with peripherals similar to conventional memory systems in a manner similar to the organization presented in [14]. This model features advanced simulation capabilities including: a) simultaneous WR on different BL, b) back-to-back RD/WR, (Fig. 2) c) evaluation of sneak current paths through inter-cell bridges d) and smart Monte-Carlo techniques with in-built response surface analysis for statistical data collection [6]. As an example, Fig. 2(a) illustrates the Write operation where the angle θ changes from π to 0 (anti-parallel to parallel). Fig. 2(b) shows the read operation from a bit-cell in the array and demonstrates an underdriven WL that reduces the probability of any inadvertant write during read (read disturb). The nominal design parameters have been summarized in Table I. We use the developed end-to-end simulation environment to study key material, device and circuit parameters and their roles in different failure mechanisms in the array.

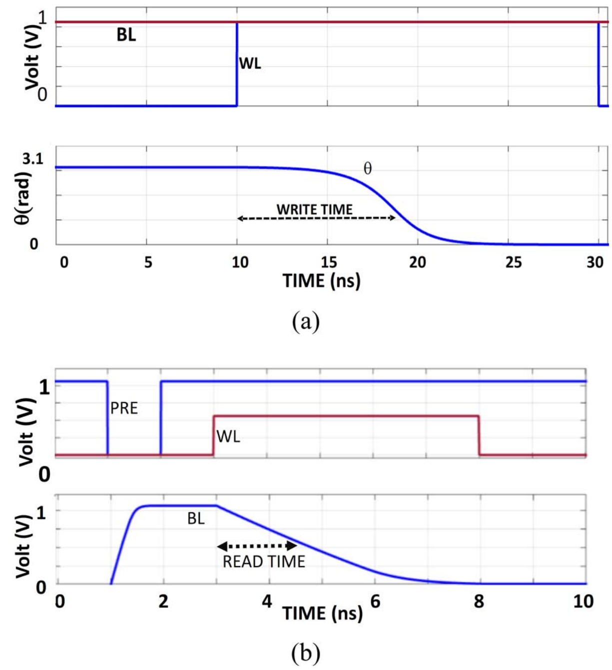


Fig. 2. Basic operations in an MTJ based STT-RAM bit-cell showing (a) write operation and (b) read operation.

TABLE I
Nominal Design and Material Parameters

	Parameter	Nominal Values
Transistor	Length	14nm
	W_access	42nm
	Fins	2
	Vth	0.25V
MTJ	Width	40nm
	Length	100nm
	Tox	1.1nm
	Ms	800 emu/cc
	RA	10
	TMR	150%
	Hk	150 Oe

IV. Paramter Variaton and Fault Models

Like every other memory technology, we expect STT-MRAM to also face process induced variations. The sources of variation in STT-MRAM bit-cells and arrays arise from process induced variations in both material and lithographic properties as well as noise generated by thermal effects. In this paper, the main sources of parametric variations that we consider are summarized as follows.

1) MTJ Material Parameters: a) normally distributed localized fluctuation of magnetic anisotropy, $\mathrm{H_K}$ [23], b) Saturation Magnetization ($\mathrm{M_S}$), c) Tunnel Magneto-Resistance ratio (TMR) which is the ratio of difference between high and low resistances to the low resistance of MTJ, all with $\sigma \sim 10\%$.

2) Transistor Electrical Parameter: a) normally distributed threshold voltage (V_t) with $\sigma \sim 10\%$.

3) Lithographic Variation: a) normally distributed variation of planar dimensions with $\sigma \sim 10\%$, and b) normally distributed variation of MgO thickness with ($\mu = 1.1$ nm and $\sigma = 0.1$ nm).

4) Thermal Fluctuations: Thermal fields lead to variation in the magnetic dynamics by a) changing the initial angle of precession and b) adding a stochastic spin torque term in LLG which causes the write times to vary [22]. The dependence of read on temperature is captured through the dependence of the resistance on temperature (5) and through read disturb, as will be discussed is Section IV-B. Retention failure is also largely dependent on the ambient temperature and is discussed in Section IV-C.

All these sources of variation lead to variations in RD, WR, and Retention. Enough guard-bands are provided in designs for a target failure probability (P_{FAIL}), typically for a 6σ corner ($P_{FAIL} \sim 10^{-9}$). Under extreme variations and defects, a particular bit-cell may fail (in RD, WR, or retention) even when design margins up to 6σ guard-bands are used. Such a failure will manifest as a fault. Hence, we need to: a) understand how large the 6σ design guard-bands are, and b) categorize the Fault Primitives and provide corresponding "Fault Models". Extreme parametric variations and/or defects during high-volume manufacturing can exceed RD, WR and Retention guard-bands, and are modeled as faults.

A. Write Operation and Failure

We first analyze the process of WR under parametric variation. A sensitivity of WR for a parameter, p is defined as $S = (\partial T_{WR}/T_{WR})/(\partial p/p)$. The sensitivity analysis of WR time with respect to key process parameters shows large dependence on the transistor threshold voltage V_{TH} and the T_{OX} of the MTJ [Fig. 3(a)]. This is followed by sensitivity on the saturation magnetization (M_S). The dependence on other parameters namely the Resistance-Area(RA) product [2] and the TMR are relatively less significant. A 6σ cell is designed using the obtained write time spread from the variation analysis. For a target storage energy Δ_{TARGET}, it is observed that the 6σ values of T_{WRITE} are 3x-4x larger than the mean [Fig. 3(b)], which is significantly larger than competing memory technologies. Considering a nominal cell with $T_{WRITE} = 20$ ns for $\Delta_{TARGET} = 60$, if a $3.5 \times T_{WRITE}$ margin is provided for the worst-case cell, from Fig. 3(b) any cell with $T_{WRITE} > 60$ ns is deemed un-writable. We characterize this as a $0 \rightarrow 1$ or $1 \rightarrow 0$ **Transition Fault (TF1 or TF0)**, where transition does not happen during the desired write window. Fig. 4 shows WR P_{FAIL} as a function of Δ for 0K and 100 °C. Apart from parametric variation, the role of temperature can also be seen here. It can be noted that higher temperature leads to a greater variability in WR time and increases the 6σ margin.

B. Read Operation and Failure

Similar analysis of RD has been performed as WR. Sensitivity of RD for a parameter p is defined as $S = (\partial T_{RD}/T_{RD})/(\partial p/p)$. The sensitivity for RD has been found to have a large dependence on the transistor threshold voltage V_{TH}, the MgO thickness T_{OX} and the TMR of the MTJ as seen in Fig. 5(a). The reliability of the Read operation is correlated with the difference in the perceived on and off resistances of the cell. These three process parameters have the maximum effect on the read time and extreme variations ($> 6\sigma$) in them lead to read failures in STT-RAM bit-cells.

1) RD Fault Models Because of Parametric Variation: The RD is characterized by two failure modes depending on the origin of the failure mode.

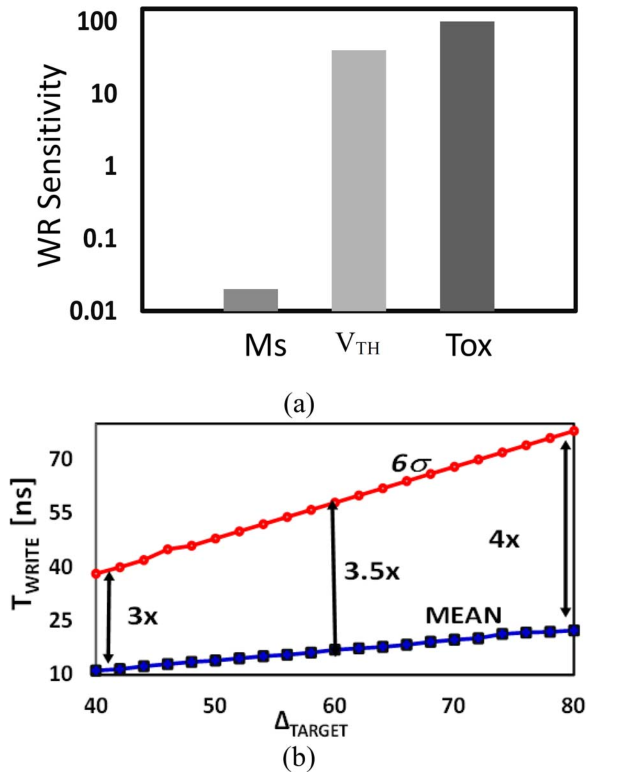


Fig. 3. (a) Sensitivity of WR time to different process and material parameters. The three main components have been shown here. The nominal WR time of the MTJ cell is 10 ns ($\Delta = 40$). (b) The WR time of a mean cell and a 6σ cell with varying Δ showing the large increase in WR time between the nominal and 6σ corners. Here $T = 0$ K is assumed.

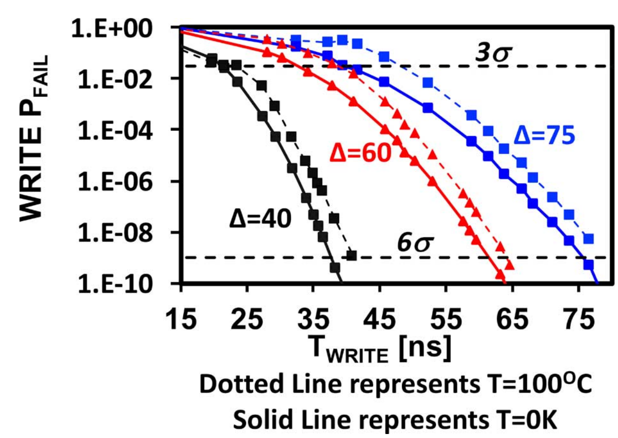
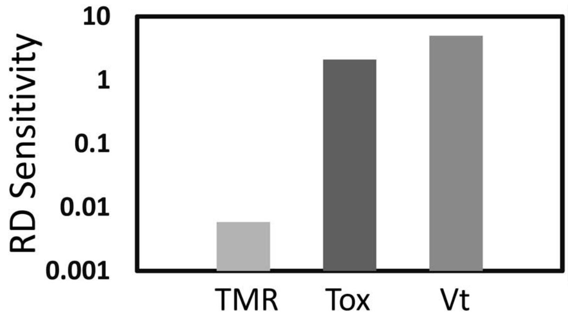
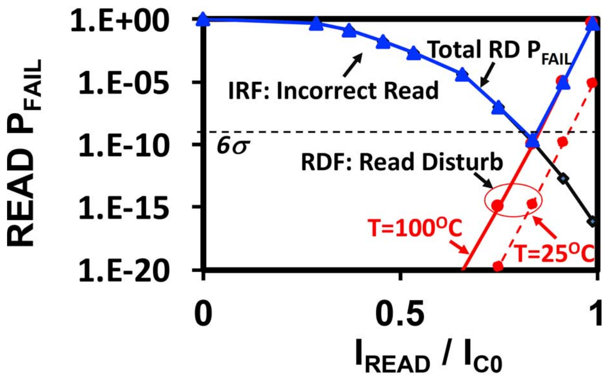


Fig. 4. WR failure probability as a function of the WR time for different target values of Δ. Simulations have been carried out at $T = 0$ and $T = 100$ °C. Higher temperature leads to a longer tail of the WR distribution and affects P_{FAIL}..



(a)



(b)

Fig. 5. (a) Sensitivity of RD time with process and material parameters. A nominal RD time of 0.5 ns has been assumed. (b) RD failure probability as a function of read current. RDF is simulated at 100 °C. RDF increases with higher temperature. IRF is calculated at 100 °C.

1) **Incorrect Read Fault (IRF):** The inability of the cell to distinguish between a '0' and '1' due to low READ current and/or low TMR [Fig. 5(b)]. The degree of impact of each parameter is again in tune to the parameter sensitivity identified earlier [Fig. 5(a)].
2) **Read Disturb Faults (RDF):** The read current for a cell is so high that the value in the cell flips during RD [Fig. 5(b)]. A lower transistor V_{TH} or lower MTJ resistance can lead to higher than nominal RD current. This can cause an inadvertent bit flip causing RDF. This is further aggravated in a weak cell whose stored internal energy (Δ) is less than a nominal target of 60. In the current study, we consider RDF in only one direction, namely a bit flip occurring when reading a stored value of 1. In Fig. 5(b) IRF is shown at 25 °C and 100 °C. Since IRF is thermal noise induced, its probability decreases with decreasing temperature and the 6σ margin needs to be characterized for the highest expected operating temperature.

C. Data Retention and Failure

Finally, a bit-cell can lose its state due to thermal noise, a problem more prominent in scaled bit-cells with decreasing Δ. Such a fault primitive is called **Retention Fault (RTF)**. Fig. 6 shows the average retention time in a nominal and a 6σ cell for varying Δ_{TARGET}, (which has been characterized at 25 °C). For seven year retention for a 6σ cell, $\Delta_{\mathrm{TARGET}} \sim 60$ is required. A comparison of Fig. 3(b) and Fig. 6 also reveals the fundamental trade-off between writability and retention.

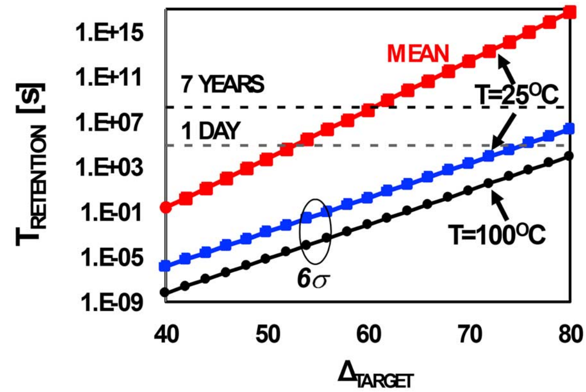


Fig. 6. Average retention time vs target Δ (that is characterized at 25 °C).

We also note a large σ/μ showing long tails in the failure probability and this is aggravated at elevated temperatures. The key fault models and parametric variations leading to these faults are summarized in Table II.

V. Defects and Fault Models

In the previous section, we have seen the role of extreme variations in different failure modes for STT-RAM. In particular, we have seen how material, device parameters and thermal effects can cause design parameters to exceed 6σ targets and cause faults in high volume manufacturing (Table II). Apart from variations, defects in the arrays are also principal sources of failures. In this section, we will consider all the possible defects inside a bit-cell and between bit-cells and their fault manifestations. Defects in a hybrid CMOS memory cell can manifest in the form of opens and shorts between various terminals [14]. Even if a cell is designed and laid out according to the design rules, there is a non-zero probability that some defects might appear during High Volume Manufacturing. [25] points out that the high resistance defects (opens) are typically caused due to salicidation, incompletely filled vias or electromigration in interconnects. Similarly, resistive shorts are also caused due to variability in the manufacturing process. In case of STT-MRAM, these defects may form during the transistor fabrication or at BEOL MTJ integration process. Authors in [12] and [13] have analyzed the various defects in SRAM array. In [13] the authors have identified static and dynamic fault models in SRAM. Similarly in [12], 18 potential defects locations in SRAM arrays have been shown. Similar defect injection and analysis methodologies have been suggested in [14] for Memristor arrays. Authors in [14] developed on this framework and provided a study of defects injected at various locations in a Memristor array identifying only the static faults. However in resistive memories such as Memristor arrays or STT-MRAM, bridge defects might occur between adjacent cells that can cause dynamic faults when two or more cells switch simultaneously. In this analysis, we focus on static faults as well as dynamic faults.

To comprehensively study all the defect models, we first categorize them as intra-cell (within a cell) and inter-cell (cell-to-cell) defects and then study their manifestation as faults. We have identified a total of 25 fault locations for injecting electrical faults for the analysis. We have also studied RC faults (not

TABLE II
FAULTS DUE TO EXTREME PARAMETRIC VARIATIONS

Fault Model	Affects	Key Cause
Transition Fault (TF)	WR	WR Time > 6σ of nominal
Incorrect Read Fault (IRF)	RD	Low TMR, low READ current
Read Disturb Fault (RDF)	RD	High RD current due to low transistor V_t, causes bit-flip
Retention Fault (RTF)	Retention	$\Delta < \Delta_{TARGET}$ with guard-band

TABLE III
DEFECT INDUCED FAULTS

Fault Model	Affects	Key Cause
Transition Fault (TF)	WR	Relative Weak WR current due to stray resistive paths
Coupling Fault(CF)	WR	Neighboring cells switching
Stuck At Fault(SF)	WR	T0 , WL stuck at VDD or GND
Incorrect Read Fault (IRF)	RD	Current miscorrelation due to defects affecting WL,BL
Read Disturb Fault (RDF)	RD	Electrical disturbance at T0 node due to larger than normal RD current

shown here) where resistive bridges were ac-coupled with parallel capacitors. However, our analysis revealed that even high capacitance values ($\sim$ fF) have negligible effect on the fault model in STT-MRAMs. Hence in the rest of the paper we will only discuss resistive defects. The resistive shorts between two nodes (*node1* and *node2*) are denoted by $\mathrm{RS}_{<\mathrm{node1}-\mathrm{node2}>}$. The high resistance opens at *node* are denoted as $\mathrm{RO}_{<\mathrm{node}>}$. In addition to the Write faults listed in Table II, defects manifest traditional fault models [13].

a) **Stuck At Fault (SF0 or SAF1):** Here resistive bridges short WL or node T0 (between transistor and MTJ) to either VDD (SF1) or GND (SF0).
b) **Coupling Fault (CF):** Here the process of WR on a neighboring cell can disturb the value in the victim. More details on the defects that can cause \CF will be discussed next. The fault models excited by defects and their key causes are summarized in Table III. We consider that Retention Failure (RTF) is not induced by resistive defects.

A. Intra-Cell Defects and Faults Models

The four terminals of the cell (BL, SL, WL, and T0, the internal node) are considered and defects and bridges are injected covering all the nodes as shown in Fig. 7(a)–(c). The opens and shorts are modeled as resistors (open: 1 kΩ to 1 MΩ and short: 10 Ω to 10 kΩ). It is observed that the identified intra-cell opens lead to faults in both 1 to 0 and 0 to 1 transitions by impeding the write current. A short explanation of each defect type and its fault manifestation is given below. The information is also succinctly summarized in Table IV.

Intra-cell opens:

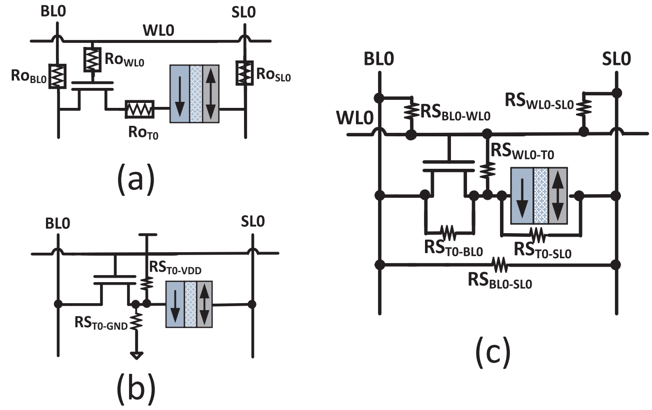


Fig. 7. Intra-cell defects: (a) opens, (b) stuck at rails (V_{DD} and GND), and (c) shorts.

TABLE IV
DEFECT AND FAULT MODELS WITH INTRA-CELL DEFECTS

Defect Type	Location	Write Fault model	Write Data Pattern (Victim)	Read Fault model	Read Data Pattern (Victim)
Open	BL0	TF0,TF1	xWx	IRF0	R0
	WL0	TF0,TF1	xWx	IRF0	R0
	SL0	TF0,TF1	xWx	IRF0	R0
	T0	TF0,TF1	xWx	IRF0	R0
Shorts	BL0 - T0		xWx	IRF1,IRF0, RDF	R1
	T0 - SL0	TF0,TF1	xWx	IRF1	R1
	WL0- BL0	TF0	xW1	RDF	R0
	WL0-T0	TF0	xW0	RDF	R0
	WL0-SL0	TF0	xW0	IRF1	R1
	BL0-SL0	TF0	xW0	IRF1	R1
	T0-VCC	SF0	xWx	IRF0	R0
	T0-GND	SF1	xWx	IRF1	R1

1) $\mathbf{RO_{BL0}}$: Degraded BL voltage leads to lower drive in 1 to 0 transitions and vice versa and leads to Transition Fault (TF). It also causes Incorrect Read Fault when a 0 is read because of insufficient BL discharge.
2) $\mathbf{RO_{WL0}}$: A weak turn on of the access transistor, affects the write current causing TF. It also causes Incorrect Read Fault when a 0 is read because of insufficient BL discharge due to lower read current.
3) $\mathbf{RO_{SL0}}$: Similar to $\mathrm{RO_{BL0}}$.
4) $\mathbf{RO_{T0}}$: This adds series resistance to the MTJ stack, resulting in lowering of write currents, causes TF. Due to low read currents, lesser BL discharge in the read time leads to IRF for Read 0 operation. It is equivalent to a SF1 as the bit-cell is always read as 1.

Intra-cell shorts:

1) $\mathbf{RS_{T0\text{-}BL0}}$: This leads to read faults (both IRF and RDF) as the WL now does not play any role in controlling the RD current through the bit-cell.

2) $\mathbf{RS_{T0\text{-}SL0}}$: Here, TF are caused in both directions because of a lower resistance path parallel to the MTJ. This shunts the WR current from the MTJ causing slower transitions or no transitions at all.
3) $\mathbf{RS_{BL0\text{-}WL0}}$: This affects transitions from 0 to 1 since WL0, which is pulled high, has a path to ground through BL0. This leads to TF. This also causes RDF because of increased WL drive.
4) $\mathbf{RS_{WL0\text{-}T0}}$: This affects transitions from 1 to 0 because of compromised WL drive and causes TF. Because of the inability of the WL to control the RD current, RDF is also increased.
5) $\mathbf{RS_{WL0\text{-}SL0}}$: This causes TF from 1 to 0 because the WL drive is weakened due of path to ground through SL0. Causes IRF1 due to slow BL discharge.
6) $\mathbf{RS_{BL0\text{-}SL0}}$: Here a short affects transition from 1 to 0 causing TF. The BL drive is weakened due to path to ground through SL0. This also leads to IRF1 due to slow BL discharge.
7) $\mathbf{RS_{T0\text{-}VCC}}$: Cell stuck at 0: Here 0 to 1 transition not possible because of zero potential difference across MTJ. The cell is always read as 0.
8) $\mathbf{RS_{T0\text{-}GND}}$: Cell stuck at 1: Here 1 to 0 transitions not possible because of zero potential difference across MTJ. The cell is always read as 1.

These defects and the WR and RD fault models they excite are shown in Table III. Here, xWy refers to a cell whose original value is x and we are trying to write y. Rx refers to reading a value of x from a cell. $x, y \in 0, 1$. xW0/xW1 refers to writing 0/1 independent of the stored value. xWx refers to any WR process on the cell.

Key Observations: For intra-cell opens, any WL open defect sensitizes the TF even for relatively small values of the defect resistance (Fig. 8). Correspondingly any short at node T0 causes TF or SAF (if the short is to V_{DD}/GND). On the other hand, shorts across the MTJ decreases RD margin (activates IRF) and across the transistor increases the RD current (causes RDF). Fig. 9 illustrates their corresponding sensitivities. Intra-cell opens increase the RD time by decreasing the RD current and cause IRF as shown in Fig. 9(a).

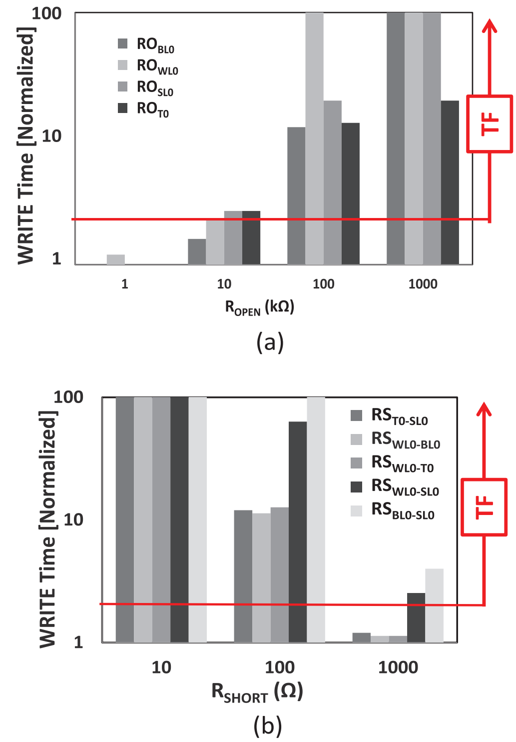


Fig. 8. Role of resistive: (a) opens from Fig. 7(a) on WR time and (b) shorts from Fig. 7(c) on WR time. Horizontal line shows the 6σ margin, above we see WR Transition Faults (TF).

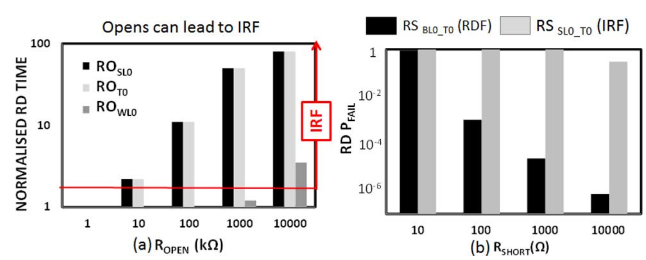


Fig. 9. (a) Resistive intra-cell opens lead to IRF where any cell whose RD time is over the 6σ margin (horizontal line) has IRF. (b) Shorts across the MTJ can cause IRF due to degraded margin whereas shorts across the transistor can cause RDF due to high current. Corresponding P_{FAIL} for RD for different values of short is shown.

B. Inter-Cell Defects and Faults Models

Inter-cell defects are associated with resistive shorts between the nodes of the victim cell and those of an aggressor cell. To study the defect and fault models, we consider a 2×2 cell array, as shown in Fig. 10. We observe the presence of 13 possible defects that can affect RD/WR of the cell. We model the faults as resistive shorts and sweep the resistance values from 10 Ω to 10 kΩ and the simulation is performed at an array level to observe the effects. The victim cell considered is cell-0 and the aggressors are cells 1, 2, or 3. In the inter-cell defects, apart from static CF's we identify dynamic faults occurring due to data dependent CF's which have not been studied in resistive memories before. These faults get activated when certain pattern is being written into the aggressor and victim cell simultaneously, causing the cell bias voltages to interact with one another and thereby compromising the drive strengths of each cell. These faults are clearly observable when the analysis is performed at a word level wherein neighborhood cells, when written together, affect each other's writability. The effect of these faults on the victim cell is described below and succinctly captured in Table V.

Inter-cell shorts:

1) $\mathbf{RS_{BL0\text{-}SL1}}$: This short causes TF when both cells are written to 0 together because of weakening of BL drive. IRF of state 0 is caused because of weak BL discharge.
2) $\mathbf{RS_{SL0\text{-}SL1}}$: This cases TF when cell-0 is written 0 and cell-1 is written 1. No effect on Read is noted as both SL0 and SL1 are connected to ground.
3) $\mathbf{RS_{SL0\text{-}BL1}}$: This leads to TF when cell-0 is written 1 and cell-1 is written 0 because the overall drive of SL0 is weakened.
4) $\mathbf{RS_{T0\text{-}WL1}}$: When WL0 is high and WL1 is low, SAF1 is caused because any drive from BL0 while writing 0 passes

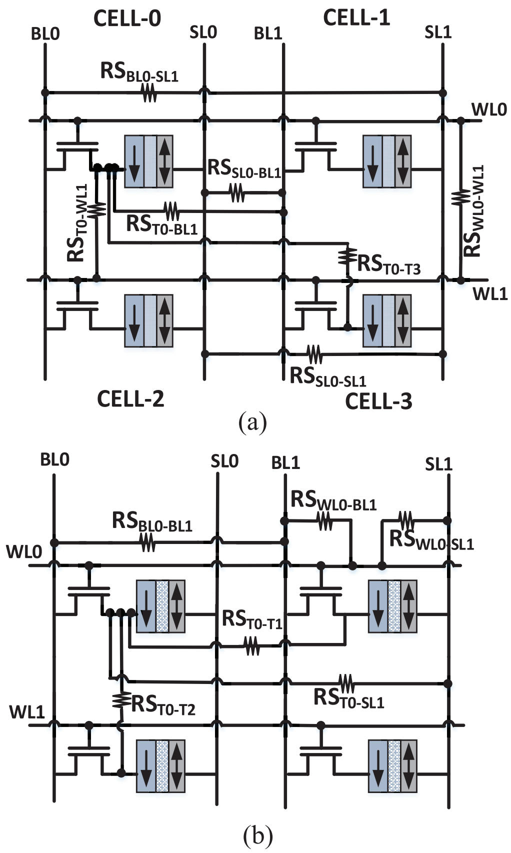


Fig. 10. Inter cell defects. Defects have been listed in Table V.

TABLE V
DEFECT AND FAULT MODELS WITH INTER-CELL DEFECTS

Location	Agressor Cell	Write Fault model	Write Data Pattern (Victim)	Write Data Pattern (Aggressor)	Read Fault model	Read Data Pattern (Victim)
BL0-SL1	1	TF0	xW0	xW0	IRF0	R0
SL0-SL1	1	TF0	xW0	xW1	No effect	NA
BL1-SL0	1	TF1	xW1	xW0	IRF0	R0
T0-WL1	1,2	SA1F,CF	xW0	Idle	IRF0	R0
T0-SL1	1	SA1F	xW0	xW0	IRF1	R1
T0-BL1	1	SA1F	xW0	xW1	IRF1	R1
T0-T1	1	SA1F,CF	xW0	xW1	RDF	R0
T0-T2	2	SA1F,CF	xW0	Idle/xW1	RDF	R0
T0-T3	3	SA1F,CF	xW0	Idle/xW1	IRF1	R1
BL0-BL1	1	TF1	xW1	xW0	IRF1	R1
WL0-BL1	1	SA1F	xW0	xW1	RDF	R0
WL0-SL1	1	SA1F	xW0	xW1	IRF0	R0
WL0-WL1	1,3	CF	xWx	Idle	IRF0	R0

to ground through WL1 rather than switching the MTJ. This causes IRF1 because of the fast discharge of BL0.

5) $\mathbf{RS_{T0\text{-}SL1}}$: This short leads to SA1F when cell-1 is written0 because the current from BL0 has a path to ground through SL1. It causes IRF1 because BL gets discharged faster.
6) $\mathbf{RS_{T0\text{-}BL1}}$: This excites SA1F when cell-1 is written1 because there is a very low potential difference across the MTJ. It causes IRF1 because BL gets discharged faster.
7) $\mathbf{RS_{T0\text{-}T1}}$: This causes SA1F when cell-0 is written0 and cell-1 is written 1 because there is a very low potential difference across the MTJ. It also leads to RDF because of coupling from cell-1 to the victim cell.
8) $\mathbf{RS_{T0\text{-}T2}}$: This leads to SA1F when cell-2 is written1 because there is a very low potential difference across the MTJ. This also leads to RDF because switching in cell-2 couples to cell-0.
9) $\mathbf{RS_{T0\text{-}T3}}$: It causes SA1F when cell-3 is written 1 because there is a very low potential difference across the victim MTJ. It also leads to IRF1 because BL gets discharged faster.
10) $\mathbf{RS_{BL0\text{-}BL1}}$: This causes TF when cell-0 is written1 and cell-1 is written 0 because the drive of BL0 is weakened due to short to ground. It also leads to IRF1 because BL0 gets discharged faster.
11) $\mathbf{RS_{WL0\text{-}BL1}}$: This causes SA1F when cell-0 is written 0 and cell-1 is written 1 because the drive of WL0 is weakened due to short to ground. Further, RDF is increased because of higher WL0 drive during Read.
12) $\mathbf{RS_{WL0\text{-}SL1}}$: This leads to SA1F when cell-0 is written 0 and cell-1 is written 0 because the drive of WL0 is weakened due to short to ground. It also leads to IRF0 because of lower WL0 drive during Read thus slower BL0 discharge.
13) $\mathbf{RS_{WL0\text{-}WL1}}$: This leads to CF when cell-0 is written 0 or 1 and cell-1 is idle the drive of WL0 is weakened due to short to ground. It also causes IRF0 because of lower WL0 drive during RD which slows down the BL0 discharge.

Key Observations: It is observed from Fig. 11 that any short involving the internal node T0 or the WL0 have a large effect on the WR time causing a TF. Defects bridging the BL0 and SL0 with neighboring cell terminals are relatively softer in impact as seen from the Fig. 11. The critical fault model is the ***data-dependent*** CF. As noted earlier, these arise in hybrid CMOS memory arrays because of the different bias conditions used for writing logic 1 and 0 and this can lead to inadvertent WR. The fault models activated with these defects and the data patterns sensitizing these faults are shown in Table V. For example, when writing 0 to both cell-0 and cell-1, if there is a bridge between BL0 and SL1 [Fig. 10(a)] this leads to weakening of BL0 possibly leading to a TF0 (transition to 0 fault). Also shorts between T0 and WL1 lead to static coupling faults where, if cell-2 is being read or written (WL1 is high), the short drives current through MTJ0 possibly switching its state inadvertently. We note that shorts to the node T0 cause CF; and the data patterns (on neighbors) which sensitize these faults are shown in Table V. Finally, a short between WL0 and WL1 can also cause both WL being simultaneously turned on (last row of Table V) causing an inadvertent WR on cell-0. Most of the inter cell defects activate IRFs. Inter cell defects occurring at T0 can potentially lead to RDF when the neighboring cell is being read or written. The short at WL0-BL1 also result in RDF as shown in Table V. It should be noted that defect analysis presented here captures the effect on nominal cells. In an already weak cell, the defects have more pronounced effects leading to faults. This is shown in Fig. 12 for representative defects. It can be compared

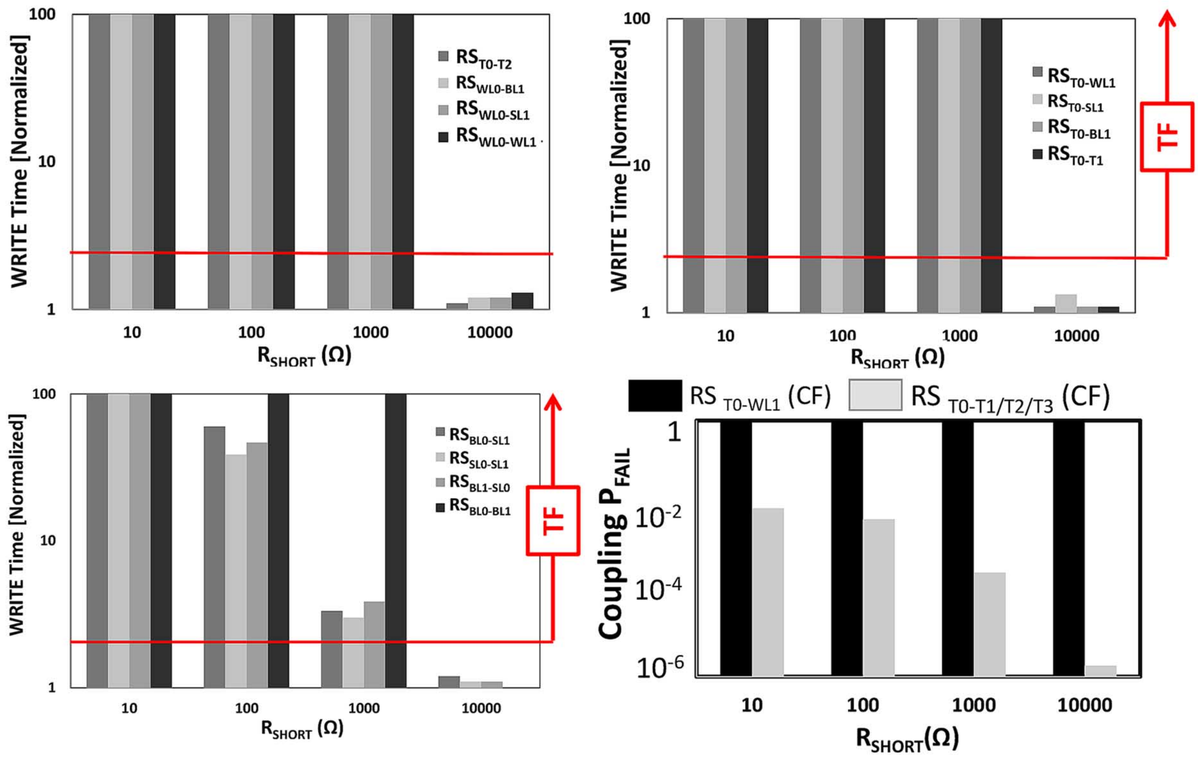


Fig. 11. Inter-cell resistive bridges activate WR TF (both TF0 and TF1 depending on the defect location). Anti-parallel cell resistance is in the order of $\sim$ 10 kΩ. Hence, any short which drains away WR current (even if the short resistance is $\sim$ k Ω) causes TF. Node T0 is most sensitive to CF and the probability of CF for T0 bridges is shown.

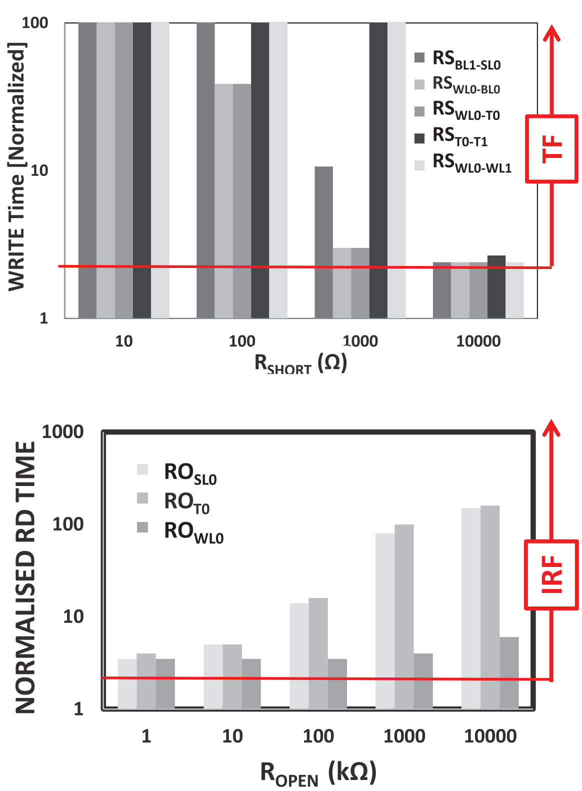


Fig. 12. Effect of defects on WR and RD for a weak (3σ) cell. We note that defects that increase WR and RD times in the nominal cell lead to faults in the weak cell.

to Figs. 8 and 9 for a comparative understanding of the role of defects in already weak (3σ) cells.

VI. Fault Excitation Through Test Pattern Generation

An analysis of defects and corresponding faults leads to the notion of test patterns and test coverage. A detailed discussion of test coverage is outside the scope of this paper, but we can compare coverage of the faults described here under existing test conditions. In particular, tests for traditional SRAM arrays and recent work on testing of resistive Memristor arrays are of interest.

Traditional RAM testing uses March tests to detect faults in an array. These have been refined over many generations of technology and in high volume manufacturing it can provide very high fault coverage. Several March tests like MATS + +, March A, March B, March C-, etc., have been proposed for SRAM arrays to detect the SAF, TF, CF fault models [26]. March C- has been shown to have a good coverage for most of these faults. These detect the static SAF, Transition and Coupling Faults in the array [26]. In STT-MRAM, for faults that have been discussed in this paper, MARCH C- can cover most of the SAF, TF, and CF. However, it is not sufficient for detecting dynamic faults that include single cell dynamic Functional Fault Models (FFMs) and Two-cell dynamic FFMs [13]. The authors in [13] have introduced March RAW and March RAW1 to detect dynamic faults for one-cell and two-cell FFMs. March RAW tests will cover dynamic faults described in Table V.

In [17] the authors have investigated new fault models in resistive arrays with Memristor based bit-cells. An existing March test (March MOM) in the context of Memristor arrays shows good coverage but the authors have noted that dynamic Write disturb fault (dWdf) is not covered by March MOM. Hence they introduced a new March test, namely March 1T-1R which covers dynamic faults in a single-cell in a Memristor. As STT-MRAM does not exhibit incremental write, the dWdf is not seen here. Also the March 1T-1R, although covers static faults and single-cell dynamic faults, the two-cell dynamic faults discussed in Section IV which involve data dependent coupling when writing two neighboring cells simultaneously are not covered. Such faults as summarized in Table V for inter-cell defects are seen when the patterns given in the table for Aggressor and Victim are written simultaneously, e.g., while writing a word. In essence, these faults are sensitized during Word level writing of the memory and thus require Word Oriented March tests for detection.

For the 2×2 array considered in this work, the word size being 2, the March RAW (Read after Write) [13] is taken and extended to the word size to detect faults given in Tables IV and V. it can be described as

$$\{\Uparrow(\mathrm{w00}, \mathrm{r00}); \Uparrow(\mathrm{w01}, \mathrm{r01}); \Downarrow(\mathrm{w10}, \mathrm{r10})\}.$$

In this current work, we have only discussed electrical defects and the corresponding faults. Magnetic field based coupling between cells may lead to Neighborhood Pattern Sensitive Faults (NPSF) that are often noted in DRAM. The origin of such faults is briefly described in [6] and is outside the scope of this current paper. Future work will enhance test coverage to include magnetic field driven NPSF.

VII. Conclusion

This paper presents a comprehensive analysis of variations and defects in STT-MRAM. Fault models corresponding to the defect models have been discussed. The results and observations will enable test pattern generation for target fault coverage.

The key observations of this work are summarized below.

1) In STT-MRAM, the parameter variations having most sensitivity for Write failure are the transistor threshold voltage, the thickness of the MgO dielectric and the saturation Magnetization of the free layer Ms. Temperature plays a key role in inducing thermal noise and it exacerbates the role of parametric variations.
2) The parameters whose variation has the most effect on Read failure probability are the transistor threshold voltage, the thickness of the MgO dielectric, and the Tunnel Magnetization Ratio.
3) The electrical defects bearing most sensitivity on Write failure probability are those occurring at the internal node T0 and those involving the Word line WL.
4) Shorts across the access transistor can cause Read disturb by flipping the bit-cell, thereby causing failure and this is exacerbated at higher temperature.
5) Shorts involving the internal node T0 can cause Incorrect Read Faults.
6) The failure probability for Read or Write gets worse in the presence of bridge defects in an already weak cell due to parameter variations, pushing errors from the soft error domain to the hard error domain where a relaxed clock frequency will not be able to recover the weak cells.
7) Bridge faults are shown to have profound effects on Write when two cells bridged by a fault are written simultaneously with a certain pattern. These faults are termed in this study as data-dependent Coupling Faults. March tests extended to a word granularity are needed to identify these faults.

The area of defect analysis and fault diagnosis in STT-RAM is an increasingly important research vector as commercialization of STT-RAM becomes a reality. As mentioned, the role of magnetic coupling and alternative device structures on defects and fault models will be addressed in future publications.

Acknowledgment

The authors would like to thank A. Parihar for fruitful discussions.

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