All-Digital Linear Regulators with Proactive and Reactive Gain-Boosting for Supply Droop Mitigation in Digital Load Circuits

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***Abstract*---This paper explores microarchitecture controlled proactive gain boosting as a means of lowering the effects of supply voltage droop in digital circuits powered by embedded, all-digital linear regulators. A behavioral power supply rejection model for all-digital linear regulator is presented. The presented regulator shows enhanced power supply rejection under increased operating frequency. Test-chip measurements in a 130nm CMOS process reveal more than 2X (4X) reduction in voltage droop (settling time) over purely reactive gain boosting.**

Keywords*---*all-digital, linear regulation, power supply rejection, proactive control.

I. INTRODUCTION

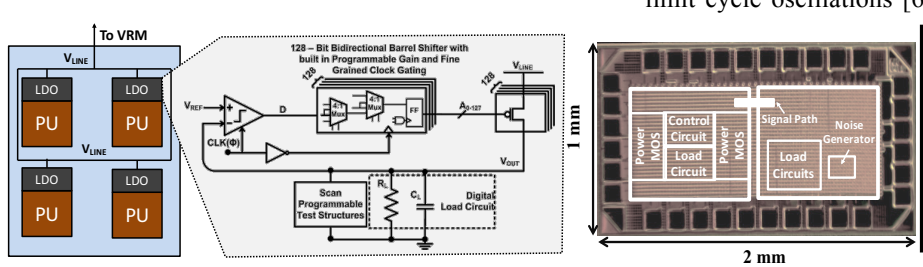
Fine-grained spatiotemporal power management in digital logic circuits [1, 2] enables higher energy efficiency through multiple power states and voltage domains (Fig. 1a). This requires innovations in on-chip Point-of-Load (PoL) linear regulators that can provide fast power state transitions, operate under large voltage ranges (from V_{MAX} to Near-Threshold-Voltage, NTV) with low decoupling capacitance and low drop-out (LDO) voltages, and exhibit stability and high current efficiency from µA to Amps of load current. Recently proposed all-digital linear regulators (Fig. 1a) [3, 4] show compatibility with the digital synthesis flow and fast response to load steps even at NTV. In spite of lower DC gain, higher ripple and lower power supply rejection (PSR), digital linear regulators provide an attractive alternative to their analog counterparts in multi-Vcc digital load circuits. Here, we explore through simulations and measurements (test-chip micrograph shown in Fig. 1b), the notion of gain-boosting through run-time operational frequency tuning in a digital regulator with reactive and proactive control [5], to minimize droops during large load steps. The major contributions of this paper are

a) Measured demonstration of the effectiveness of proactive software control to enhance LDO transient performance under large voltage droops.
b) PSR modeling of all-digital LDOs and gain boosting to enhance PSR performance against supply noise.

After a brief introduction in Section I, the design and general trade-offs of an all-digital linear regulator are discussed in Section II. A comparison of reactive and proactive control for mitigating power supply rejection is carried out in Section III. Section IV presents a power supply rejection model used to analyze the underlying regulator and performance adaptation through gain boosting. Both Section III and IV provide measurement results from the test chip. Finally, the manuscript is concluded in Section V.

II. DIGITAL LINEAR REGULATORS

A dual clock edge all-digital LDO is presented in Fig. 1a. The design consists of a digital control section comprising of a clocked comparator followed by a shift register and an array of 128 controlled PMOS pass devices. The second-order closed loop gain of the LDO is a function of the sampling clock frequency (F_S), as has been discussed extensively in [3,6]. The design of the LDO follows a topology as described in [6]. An increasing F_S (relative to the location of the output pole, $F_{LOAD}=1/2\pi(R_{LOAD}.C_{LOAD})$), takes the system from an over-damped to the underdamped response. Further, the hard quantization of the comparator and the finite quantization of the PMOS array introduce steady-state limit cycle oscillations [6] and hence an output ripple,



(a) (b)

Technology	130 nm
Package	32 pin QFN
V_{IN}	0.5 - 1.2
V_{OUT}	0.45 - 1.14
I_{OUT} (max)	4.6 mA
Load Regulation	<10 mV/mA
Power Supply Rejection	> 7.6 dB
LDO area	0.144 mm^2
chip area	2 mm^2

(c)

Fig. 1: (a) Multiple on-chip power domains with embedded point-of-load digital LDOs. (b) Chip micrograph showing two voltage domains. (c) Chip specification table

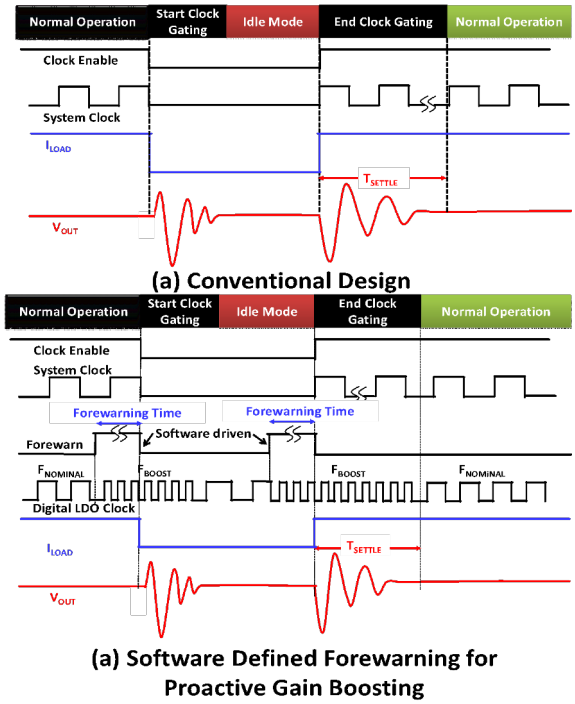


Fig. 2: (a) Conventional design showing supply droops/overshoots in response to clock gating/un-gating. (b) Forewarning signal provides proactive gain boosting in digital regulators.

which is a hallmark of digital regulators. A higher F_S increases the limit cycle oscillation which can lead to higher steady-state ripple; hence, *the ratio of F_S/F_{LOAD} needs to be bounded*. In the current design a nominal F_S ($F_{NOMINAL}$) of 20MHz was selected. Since F_S plays a critical role in the overall closed-loop gain of the system, it also provides a unique opportunity to enable real-time and 'almost instantaneous' gain boosting in a digital regulator in response to a large load step. In this paper, we explore such a paradigm through measurements on a silicon chip fabricated in a CMOS 130nm IBM process (Fig. 1b, c) and demonstrate the efficacy of gain boosting in digital regulators. Clock gating, an effective method of power saving in digital load circuits, is commonly used in industrial designs. However, going into (coming out of) a clock gated mode from (to) normal operation, creates very large load transients and lead to large overshoots (voltage droops) in the logic circuit (Fig. 2a). The corresponding response time of the supply regulator, hence, is critical, and limits how often clock gating can be employed.

IV. PROACTIVE VS REACTIVE CONTROL

In traditional design, regulators (analog or digital) are feedback circuits that react to changes in the output voltage by regulating the current to the load. A higher closed loop gain (within the bounds of stability) can achieve faster regulation. Unlike analog regulators, in a digital regulator, the loop dynamics (particularly gain and system poles) can be controlled by F_S [6], and sudden current demands can be satisfied by gain-boosting even at low currents (voltages). In our design, gain boosting is achieved by employing an undershoot and overshoot detector which compares the output voltage with $V_{REF}\pm\Delta$ such that whenever an undershoot or overshoot is detected, a higher F_S is employed and a faster recovery and lower supply droop/overshoot is achieved at iso-load step (Fig. 3). Test-chip measurements of such a reactive scheme demonstrate significant improvements in both the transient time and magnitude of the droop for different values of Δ, for two different values of the boosted regulator frequency (F_{BOOST}) (Fig. 4a, b). As opposed to this purely reactive scheme, a '*load-regulator co-design*' can enable a proactive approach in droop mitigation. In most digital designs, information about large transient events, like clock gating/un-gating is available a few clock cycles in advance from the microarchitecture/software stack [8, 9]. Clock gating during a cache miss in a microprocessor, or refreshing a display in a mobile device are examples of workloads with very predictable and deterministic clock gating/un-gating patterns. Since the microarchitecture state is expected to have visibility into the system over several clock cycles, a forewarning signal can be issued before the actual clock gating/un-gating is enabled. Such a forewarning signal can be propagated to the digital LDO in a feed-forward path. It can, then, allow the regulator to preemptively switch to higher gain, to reduce an impending voltage droop. The earlier this warning signal is propagated to the LDO, the lesser the droop and the settling times are (Fig. 4c,d). From silicon measurements, we note a saturating trend when the warning signal is available more than 100ns in advance. We see large benefits with a forewarning signal that arrives 10ns-100ns before the actual load step, which is equivalent to 10-100 clock cycles in a 1GHz processor and is in the realm of prediction from the microarchitecture [9].

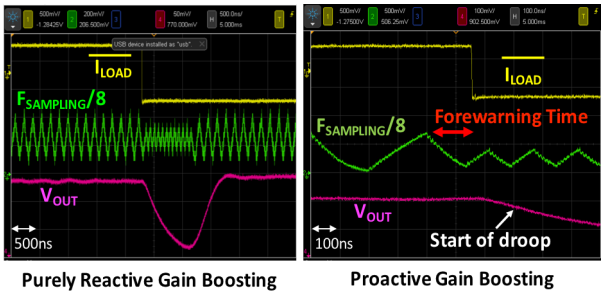


Fig. 3: Oscilloscope captures showing purely reactive and proactive gain boosting under iso-load steps (2mA step). Here $F_{SAMPLING}=F_S$ has a nominal value of 20MHz.

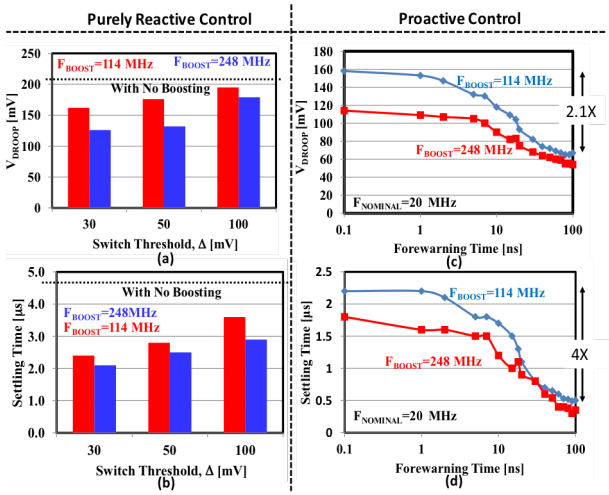


Fig. 4: (a-b) Measured droop reduction and settling time for reactive control. (c-d) Measured droop reduction and settling time at iso load-step conditions. The nominal F_S is called $F_{NOMINAL}$.

III. POWER SUPPLY REJECTION AND GAIN-BOOSTING TO REDUCE CROSS-DOMAIN SUPPLY NOISE

In digital linear regulators, the power MOSFETs operate in a linear or triode region. This leads to a lower power supply rejection (PSR), which is typically an acceptable trade-off in digital load circuits. However, this leads to cross-domain noise coupling where supply noise of a local grid can propagate through a shared line voltage (Fig. 1) to adjacent grids. In this section, we demonstrate (through theory and measurements) that the poor PSR in digital LDOs can be compensated for by proactive gain boosting in adjacent (victim) power grids when a large load transient in expected in an aggressor power grid. A behavioral model to explain PSR can be best approximated in the steady state where all the 'on' switches of the PMOS array are contributing equal current to the output under a constant drop-out voltage. Under such conditions, following the PSR shunt model of [7], we can model the Z_{OUT} at the output of the LDO as a parallel combination of shunt (≈ Z_{OUT}/loop gain (LG)) and load impedances. Increasing F_S increases LG which lowers the shunt impedance and steers the noise current away from the load. At a decreased F_S, the effect of shunting impedance is reduced which decreases the closed loop gain and lowers the PSR.

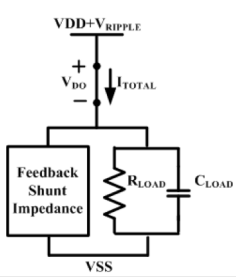


Fig. 5: PSR model showing shunt feedback path.

A. Power Supply Rejection Model

In this subsection, we provide a mathematical framework which establishes the effect of increasing F_S on the power supply rejection performance of a digital LDO. With a constant feedback factor (=*1*) and load (F_{LOAD}), following the analysis carried out in [10], LG of the LDO in z-domain is given as

$$LG(z) = \frac{K(1-e^{-F_{LOAD}/F_S})}{(z-1)(z-e^{-F_{LOAD}/F_S})} \quad (1)$$

Here K comes out to be a constant of proportionality which represents the gain of PMOS devices. Under the constraint that F_S is at least 5 to 10 times higher than F_{LOAD} [3], a z-domain to s-domain transformation is used:

$$z = 1 + s(T_S) \quad (2)$$

where $T_S = 1/F_S$. Putting (2) in (1) gives

$$LG(s) = \frac{K(1-e^{-F_{LOAD}/F_S})}{(sT_S)(1+sT_S-e^{-F_{LOAD}/F_S})} \quad (3)$$

$$LG(s) = \frac{K}{(sT_S)\left(1+\frac{sT_S}{1-e^{-F_{LOAD}/F_S}}\right)} \quad (4)$$

By Taylor's expansion and neglecting higher order terms, $e^{-F_{LOAD}T_S} \approx 1 - F_{LOAD}T_S$. Then (4) can be written as

$$LG(s) = \frac{K}{(sT_S)\left(1+\frac{s}{F_{LOAD}}\right)} \quad (5)$$

PSR analysis is divided in to two different frequency regions. Region I: In the first region $s > 2\pi F_{LOAD}$ and Region II: where $s < 2\pi F_{LOAD}$. Following Fig. 5 [7], impedance looking downward into the load at the regulated output voltage is given as:

$$Z_{PD} = Z_{LOAD} || Z_{SHUNT} \quad (6)$$

$$Z_{PD} = \frac{R_{LOAD}}{1+s/F_{LOAD}} || \left[\left(\frac{R_{LOAD}}{1+s/F_{LOAD}} || \frac{V_{DROPOUT}}{I_{LOAD}}\right)/LG\right] \quad (7)$$

In region I, value of LG is small as can be inferred from (5), therefore; Z_{PD} is dominated by the output pole. In this region, C_{LOAD} shunts away the ripple noise. In region II, equation (5) is used in (7) under the assumption that $s << 2\pi F_{LOAD}$. It results in the following simplified form of pull down impedance:

$$Z_{PD} = R_{LOAD} || \left(\left(\frac{V_{DO}}{K\ VDD}\right)(sT_S)\ R_{LOAD}\right) \quad (8)$$

From (8), it can be clearly inferred that with decreasing T_S, Z_{SHUNT} becomes smaller than Z_{LOAD} and shunts away

the ripple current coming to the regulated output node from the supply. The PSR of the system is given as:

$$PSR = \frac{Z_{PD}}{Z_{PD} + R_{DO}} \quad (9)$$

which shows that decreasing Z_{PD} improves power supply rejection at low frequencies at higher F_S. This is corroborated through measurements as described below.

B. Cross Domain Proactive Regulation

With an injected supply noise of 85mV p-p, a measured PSR of 7.61dB is achieved when the system is running at an F_S of 54 MHz and I_{LOAD} of 2mA (Fig. 6a). As Fs is further increased the output noise falls below the noise floor caused by the steady state ripple [6]. An unwanted consequence of this, in a multicore processor, is that load transients (due to clock gating/un-gating) from one core can cause large voltage fluctuations in the shared incoming voltage grid. The noise predominantly spreads at the resonant frequencies of the LC section of the package and the package to chip interface. Due to the poor PSR of digital linear regulators, a large portion of the noise can couple into adjacent cores (which are running workloads) creating timing errors. The availability of a forewarning signal before clock gating/un-gating can also be propagated to adjacent voltage grids to temporarily boost the local regulator clock (F_S) and provide an instantaneous boost in the PSR. This opportunistic PSR adaptation comes at a minimal cost of increasing F_S only during large load transitions. It reduces the magnitude of the coupled noise and time to recover from the noise. With warning signal propagated 10 ns in advance to a noise event occurring in an adjacent load, the proactive gain boosting achieves a 3X decrease in settling time and a 2X decrease in voltage droop magnitude. If the forewarning signal is available well in advanced (> 10 ns) the transient performance of gain boosting saturates since the system is already operating at its highest rated performance. The measured results from the test chip showing the efficacy of this run time adaptation are summarized in Fig. 6 (b,c).

IV. CONCLUSION

This paper demonstrates the effectiveness of proactive, software-defined control in digital, embedded linear regulators to minimize the effects of supply droops and coupling noise by instantaneously boosting the regulator's sampling frequency. Increased operational frequency of the regulator under varying load conditions can help achieve on demand power supply rejection improvement. PSR of the system is modeled analytically and measurements from a test-chip are provided to prove the efficacy of proactive supply drop mitigation and validation of the PSR behavior.

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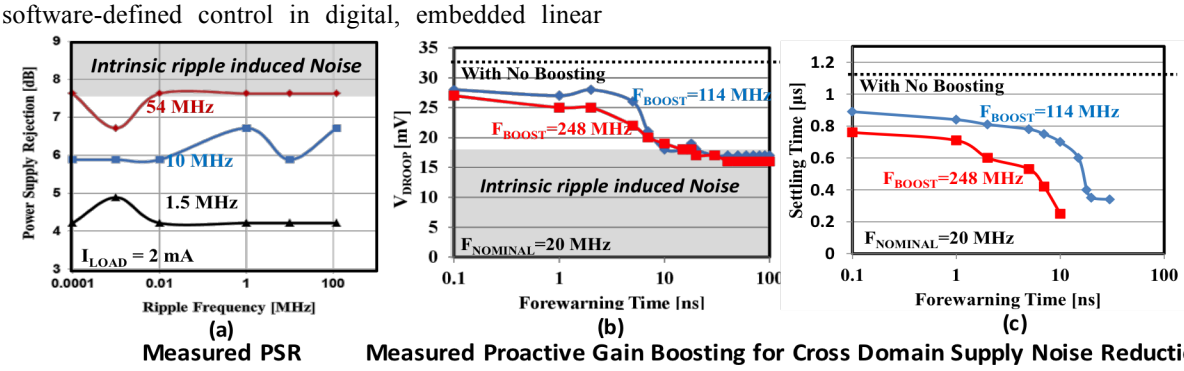

Fig. 6: (a) Measured PSR as a function of ripple and sampling frequencies illustrates low overall PSR in digital regulators. (b) Measured voltage droop and settling time as a function of the forewarning time shows large improvement in mitigating cross-domain supply noise.