Phase Transition Oxide Neuron for Spiking Neural Networks

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Introduction: Spiking neural networks are expected to play a vital role in realizing ultra-low power hardware for computer vision applications [1]. While the algorithmic efficiency is promising, their solid-state implementation with traditional CMOS transistors lead to area expensive solutions. Transistors are typically designed and optimized to perform as switches and do not naturally exhibit the dynamical properties of neurons. In this work, we harness the abrupt insulator-to-metal transition (IMT) in a prototypical IMT material, vanadium dioxide (VO_2) [2], to experimentally demonstrate a compact integrate and fire spiking neuron [3]. Further, we show multiple spiking dynamics of the neuron relevant to implementing 'winner take all' max pooling layers employed in image processing pipelines.

Experiment: Figure 1 shows a schematic of the VO_2 spiking neuron consisting of a transistor in series with VO_2 integrated on the drain terminal. The operating principal of this spiking neuron is shown in Figure 2(a), wherein initially the membrane potential is raised by an incoming spike at time t. The potential persists for a time, Δt, decaying slowly until either another incoming spike raises the potential again or the potential returns to the rest state (u_{rest}). When the membrane potential reaches the threshold value, u_{th} (activation potential), the neuron fires a spike. The mathematical equation governing this leaky integrate and fire neuron is shown in the inset Figure 2(c). This functionality can be demonstrated using the equivalent circuit in Figure 2(c) due to electrically accessible conductance oscillations in VO_2 which produce neural firing at the output for a range of transistor gate voltages [4]. The conductance oscillations in VO_2 occur when the transistor load line intersects the unstable arms of the DC I-V in Figure 2(e); else no oscillations are present (Figure 2(d)) [5]. The temporal response of the neuron using a 6μm x 6μm planar VO_2 device and silicon MOSFET is shown in Fig. 3. As the input spikes raise the membrane potential above u_{th} spiking occurs at the output (V_{out}) until the membrane potential subsides below u_{th}. To implement a leaky integrator for the neuron a low pass filter is placed at the transistor gate terminal. This functionality is highlighted in Fig. 4 where the input voltage is integrated across ten input cycles for the activation potential to be reached, after which the neuron begins to fire. Additionally, the VO_2 neuron exhibits frequency adaptation as displayed in Fig. 5 where the spike frequency increases with gate voltage. Finally, we demonstrate neural inhibition in Figure 6 wherein two neurons are placed in a feedback loop such that the output of the second neuron turns on a secondary transistor parallel to the VO_2 in the primary neuron, preventing the primary neuron from firing (red). Such inhibition, frequency adaptation, and integrate and fire responses can be used to implement winner-take-all max pooling layers extensively deployed in image processing tasks in neural networks. Figure 7 illustrates the structure of such a layer, where three neurons receive signals of varying strength (frequency) and only the winner neuron fires.

Conclusion: In summary, we demonstrate a compact spiking neuron based on the insulator-to-metal electronic phase transition in VO_2. The device maps to a standard leaky integrate and fire model and is capable of producing a gamut of spiking dynamics including integrate and fire, frequency adaptation, and inhibition. These spiking dynamics are relevant to winner-take-all max pooling layers for use in image processing tasks.
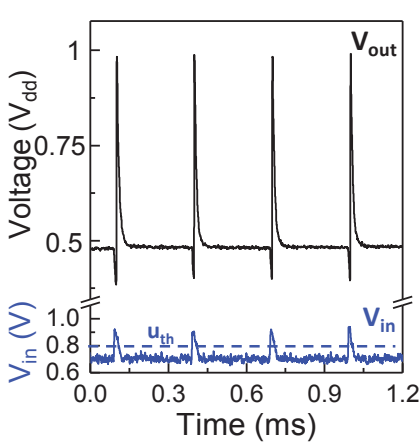
References: [1] P. A. Merolla, et. al., *Science*, vol. 345, no. 6197, pp. 668-673, 2014. [2] L. A. Ladd et. al., *Solid State Commun.*, vol. 7, no. 4, pp. 425-428. [3] E. M. Izhikevich, *IEEE Trans. Neural Networks*, vol. 15, no. 5, pp. 1063–1070, 2004. [4] W. -Y. Tsai, et. al., *IEEE Trans. Multi-Scale Comput. Syst.*, pp. 1-1, 2016. [5] N. Shukla, et. al., *Sci. Rep.*, vol. 4, p. 4964, Jan. 2014.
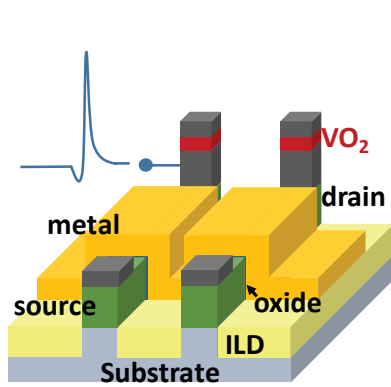
Fig.1: Schematic of IMT neuron. VO$_2$ is placed in series with Silicon transistor at the drain which shows spiking behavior.
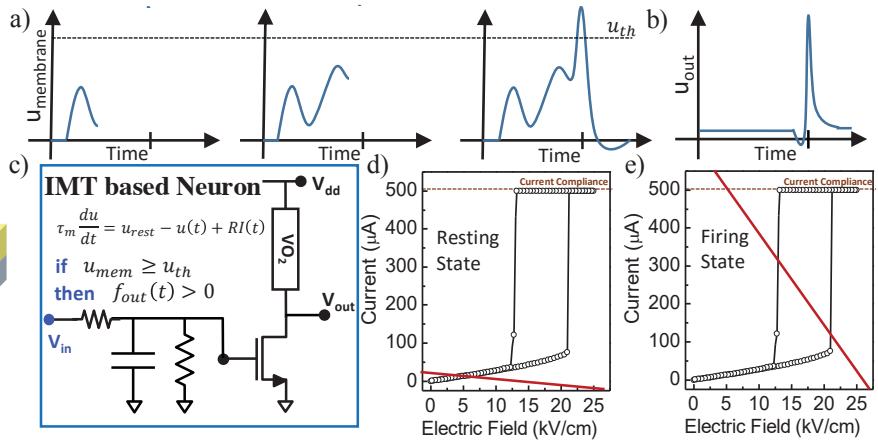
Fig.2: (a-b) Neuron characteristics: (a) Membrane potential is slowly raised by integration of input spikes until the activation potential (u$_{th}$) is reached and (b) a spike is produced at the output. (c) Leaky integrate and fire equation and IMT based neuron implementation where neural firing results from conductance oscillations in VO$_2$. (d) Resting state load line. (e) Firing state load line.

IMT based Neuron

$$\tau_m \frac{du}{dt} = u_{rest} - u(t) + RI(t)$$

$$\text{if} \quad u_{mem} \geq u_{th}$$
$$\text{then} \quad f_{out}(t) > 0$$

Fig.3: Response of VO$_2$ neuron in both resting and firing states. As the input rises above the activation potential (u$_{th}$), firing occurs.
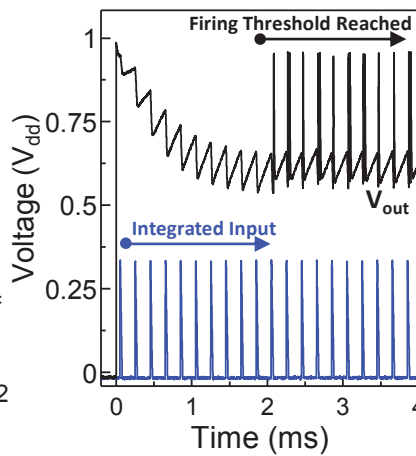
Fig.4: Demonstration of integrate and fire in a VO$_2$ neuron. The membrane potential is raised until threshold is reached and the neuron begins to fire.
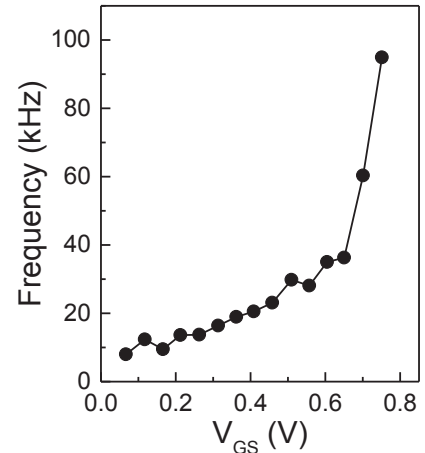
Fig.5: VO$_2$ neuron exhibiting frequency adaptation as a function of the gate voltage. Frequency is tunable over one order of magnitude.
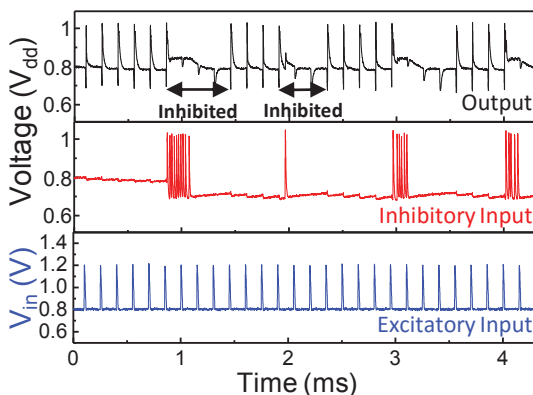
Fig.6: Temporal response of inter neuron inhibition. The response of the principal neuron (in black) and the inter neuron (in red) in response to excitatory input (in blue).
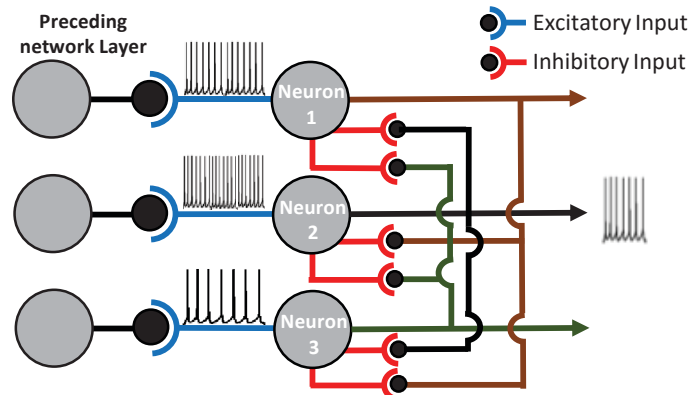
Fig.7: Schematic for implementation of winner-take-all max pooling layers for computer vision applications. Incoming signal from preceding network layer feed the principal neurons which feedback to the each other through inhibitory inputs.