A 130nm Hybrid Low Dropout Regulator based on Switched Mode Control for Digital Load Circuits

Saad Bin Nasir, Shreyas Sen* and Arijit Raychowdhury
Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA, USA
* Electrical and Computer Engineering, Purdue University, West Lafayette, IN, USA
saadbinnasir@gatech.edu, shreyas@purdue.edu, arijit.raychowdhury@ece.gatech.edu

Abstract— **A hybrid (digital and analog) low dropout regulator (LDO) utilizing switched mode control is designed in 130 nm CMOS for fine grain power management, fast droop recovery and robust small signal regulation of multi-V_{CC} digital loads. The design provides an optimal trade-off of performance and accuracy by switching between a digital and an analog control loop. The hybrid topology achieves robust small signal regulation and fast recovery from large signal transients or power state transitions. Measurements from a 130nm test-chip show Near-Threshold Voltage (NTV) operation, fast transient response of 18 ns for a load step of 10.3mA and a peak current efficiency of 98.64%.**

I. Introduction

On-chip voltage regulation is becoming necessary to reduce power delivery path losses, handle wide-scale workload variations and large load transitions in digital circuits [1]. Integration of low dropout (LDO) regulators at the point of load (PoL) help address these challenges. As a result, the performance requirement on these PoL LDOs is becoming unexpectedly high under strict power constraints. Traditionally, analog LDOs have been employed for voltage sensitive analog load circuits which typically represent, mostly, DC loads. On the other hand, digital load circuits exhibit large load transients and wide operating voltages (from V_{MAX} to Near-Threshold Voltages, NTV). Hence, linear regulators (including LDOs) that supply digital loads have a different value proposition, such as the capacity to operate at wide operating voltages and respond to large load steps. This is particularly true when the underlying load circuit is in a low-current/low-power state and needs to wake up in a few clock cycles. Other conventional metrics of analog LDOs, like voltage ripple, PSR can be relaxed as these non-idealities add a small margin to the already existing voltage guard-band due to temperature, process and aging variations. To address these challenges of power delivery for digital load circuits, this manuscript makes the following contributions:

- Exploit the recent advances of the theory of ***Switched Mode Control (SMC)*** to decouple Large Signal (LS) performance from Small Signal (SS) regulation.
- Combining ***analog LDO for SS regulation*** and a ***digital LDO for LS transient performance*** in a hybrid topology, thereby providing an optimal design solution.
- Take advantage of the novel, active load-sharing in SMC to design a ***fully integrated and capacitor-less output pole dominant (OPD) analog LDO***, thus inheriting the wide bandwidth and gain of OPD analog LDOs.

The paper is organized as follows. Limitations of current topologies to address regulation of digital load circuits are elaborated in Section II. A detailed architecture of the proposed hybrid LDO is discussed in section III. It is followed by circuit level implementation details in section IV. Measurement results from a 130 nm test-chip are provided in section V, followed by conclusion.

II. Limitations of current solutions

Both analog and digital LDOs are being researched to meet the growing challenge of providing fast, energy efficient and wide operational voltage range; but they have their own strengths and weaknesses. Analog LDOs show tight SS regulation, but lack voltage scalability and ability to handle large current transients [2]. Whereas, digital LDOs show fast LS performance but lack SS regulation [3-6], have steady state ripple and consume clocking and dynamic power in steady state. To overcome some of these limitations, dual loop LDO architectures have been proposed. In these topologies, multiple feedback loops work in tandem to achieve regulation. Most of them comprise of completely analog solutions [1,2,7] with a recent demonstration of a dual loop digital LDO [8]. In these topologies, the operation of the loops is divided across different frequency regions to maintain stability. SS gain and bandwidth increases in these topologies at the cost of higher controller power. Since the LS loop is operating simultaneously with the SS loop, its gain and bandwidth are limited to maintain stability and good SS performance [1,7]. Although the dual loop digital LDOs provide fast transient response but they suffer from the same steady state limitations (existence of limit cycles and low SS gain) as that of a single loop digital LDO [3,8].

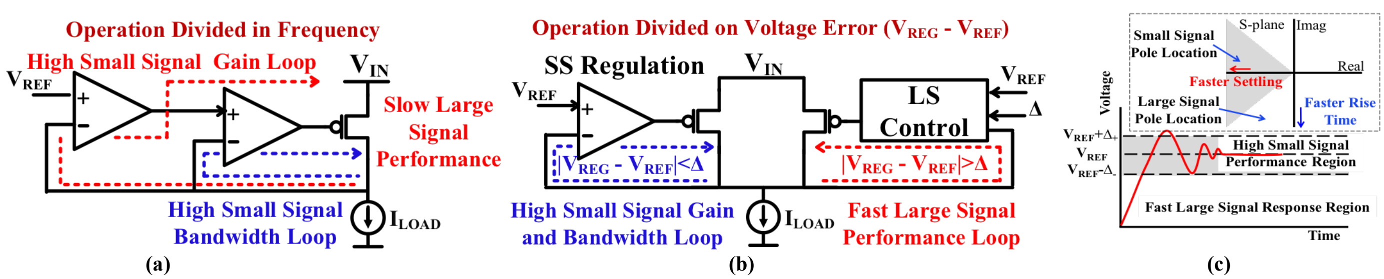


Fig. 1. Comparison of dual loop topologies (a) Prior. (b) Proposed. (c) Location of system closed loop poles to achieve optimal small signal and large signal performance.

The work was funded by SRC through the Texas Analog Center (Task # 1836.180), Qualcomm Inc. and Intel Corp and NSF CRII Grant 1464353.

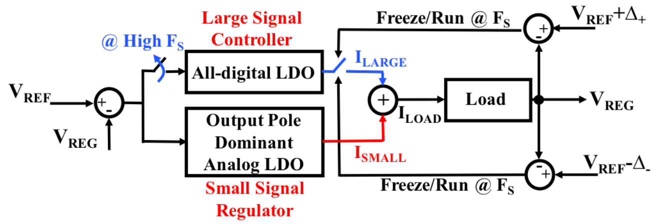


Fig. 2. Feedback control schematic of the proposed hybrid LDO.

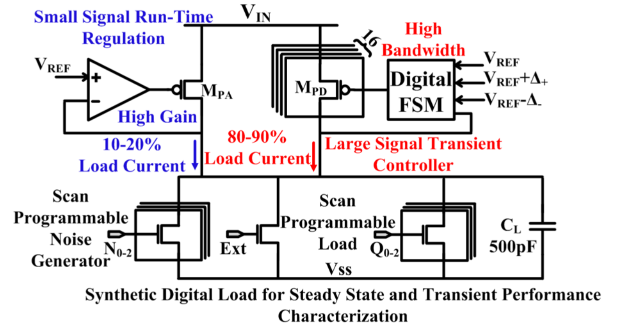


Fig. 3. Hybrid LDO system architecture.

TABLE I. LARGE SIGNAL CONTROLLER AND SMALL SIGNAL REGULATOR SELECTION

LS LDO Topology Characterization			SS Analog LDO Topology Characterization		
Type of LDO	Analog	Digital	Dominant Pole Location	Internal	Output
Rise Time	Slow	Fast	V_{DROOP}	High	Low
Closed Loop Control	High	Low	PSR	Low	High
Process Scalability	Low	High	UGF	Low	High
Design Complexity	High	Low	Light Load Stability	No	Yes
Performance Adaptation	Low	High	On chip Integration	Standard	Difficult
Design Choice		✔	Design Choice		✔

III. Hybrid LDO Design Architecture

SMC Fundamentals: To achieve both fast LS performance and robust SS regulation, we propose a hybrid LDO, which uses switched mode control (SMC) to combine the strengths of both analog and digital LDOs. The proposed design decouples the SS gain from LS transient response by utilizing a voltage based error signal (V_{REF}-V_{REG}) to switch from one controller to another. This is fundamentally different from other dual loop architectures, which utilize both the loops simultaneously throughout the regulation as differentiated in Fig. 1a and 1b. The presented SMC is a unique control topology in which a closed loop controller discretely switches from one control law to another, depending on the magnitude of the loop error. The regulator classifies voltage error (V_{REF}-V_{REG}) as either LS (|error|>Δ) or SS (|error|<Δ) to switch between two optimal controllers. Optimality criterion for LS region is fast rise time (T_{RISE}). For SS region, it is fast settling time ($T_{SETTLING}$). SMC allows the two separate optimal controllers to be combined together, by switching at a threshold, to achieve an overall optimal response to LS transients. Location of the dominant pole of the overall system for each controller determines its response as illustrated in Fig. 1c. For a fast LS response, the dominant poles of the system should have low damping, which allows faster rise times. Whereas, a faster settling time is achieved by placing the dominant poles of the system deep in the left half s-plane. LS is separated from SS region by a voltage dead-zone established by two thresholds, Δ_+ and Δ_-, above and below V_{REG}. SS controller is enabled when V_{REG} is within this dead-zone. Since LS controller operates across a large V_{REG} region, it is designed to fulfill most of the load current requirement (power transistors are sized to provide 80-90% of load current at maximum current rating). Therefore, instead of turning off LS controller in the dead-zone, its state is frozen. This mechanism not only helps deliver most of the load current requirement through LS controller but also prevents switching noise. Similarly, to prevent SS regulator switching noise, it is always kept on. The high operational BW (explained later) of the LS controller is used to make SS regulator ineffective when V_{REG} is out of the dead-zone. A control schematic of the complete system is shown in Fig. 2.

Choice of analog vs. digital for SS and LS Control: This brings us to the question of the choice of regulator topology for each region. As summarized in Table. I, a higher integration density, process scalability, and most importantly, ultra fast response without slew limitation, makes digital LDO an ideal choice to act as the LS controller. Further, a digital LDO can be adaptively made severely underdamped with a fast operational clock frequency [3] as desired for the LS controller. For SS controller, a small quiescent power consumption, high SS gain, and ripple-free SS response makes analog LDO the design choice. Analog LDOs can be further divided in to two major categories (Table I). Internal pole dominant (IPD) and Output pole dominant (OPD) LDOs. OPD analog LDOs offer better power supply noise rejection, faster droop compensation, and light load stability compared to their IPD counterparts. Therefore, the SS controller design choice should be an OPD analog LDO. Conventionally, a small on-die capacitance budget limits its use in PoL voltage regulation. OPD analog LDO loses its phase margin (PM) with increasing load currents at a given output capacitance. The presented hybrid topology overcomes this integration challenge by using LS controller to deliver most of the load current. It allows the synthesis of an analog LDO, which delivers a small portion of the total current (10-20% of total load current at maximum current rating). This requires a smaller power MOSFET which pushes the internal pole of the loop to a high frequency (to be discussed in Section IVB). Hence, we can have a ***stable OPD analog SS loop*** and maintain a high PM, throughout the operational current range. For a voltage undershoot, the LS digital LDO turns on power transistor array in a thermometer fashion until V_{REG} reaches V_{REF}-Δ_-. Once V_{REG} enters the dead-zone, LS controller is

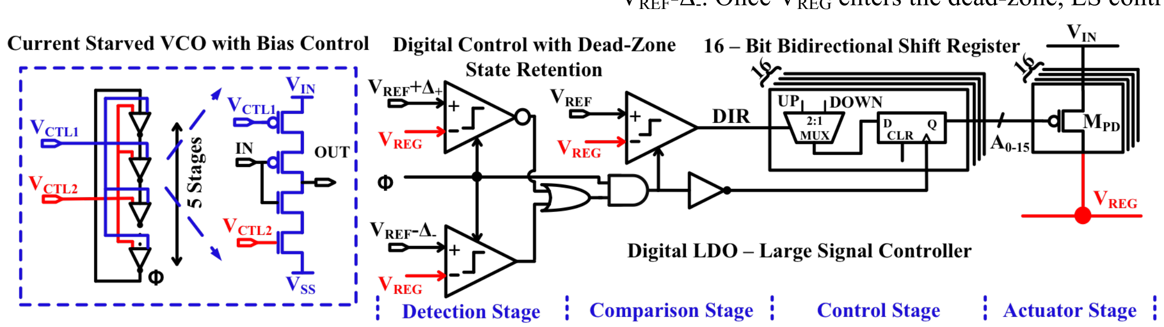
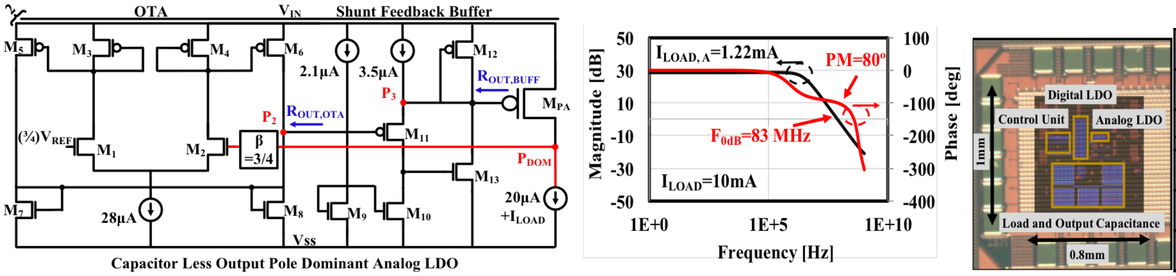


Fig. 4. Large Signal (LS) Controller with clock generation through a 5 stage current starved voltage controlled oscillator.



Process	GF 130nm CMOS
Package	QFN
Active Area	0.0818mm²
V_{IN}	0.6V, 1.1-1.2V
I_{LOAD}	30µA – 12mA
V_{OUT}	0.5-0.55V, 0.8-1.1V

(a) (b) (c)

Fig. 5. (a) Output pole dominant (OPD) analog LDO as the SS Regulator. (b) Simulated Phase Margin at V_{REG}=1V. (c) Die micrograph with characteristics

frozen and the SS regulator provides the remaining load current and brings V_{REG} to V_{REF}. For an overshoot, $V_{REG}+\Delta_+$ acts as the dead-zone boundary with SS regulator operational when $V_{REG}<V_{REF}+\Delta_+$. The choice of switching thresholds ($\Delta-$, $\Delta+$) not only ensure stable operation (no chattering between the two controllers) but also help ensure optimal current delivery to the load. Since the presented LS digital LDO is synchronous and capable of operating at a high frequency reaching up to 900 MHz, it has a higher bandwidth and provides all the load current, unless its state is frozen. A digital LDO, on the other hand cannot be stable at such high frequencies without the dead-zone, as we demonstrated in [3]. Therefore, there is no need to explicitly turn off the SS regulator when $V_{REF}-V_{REG}>|\Delta|$. A complete system architecture of the presented hybrid LDO is shown in Fig. 3.

IV. Hybrid LDO Circuit Implementation

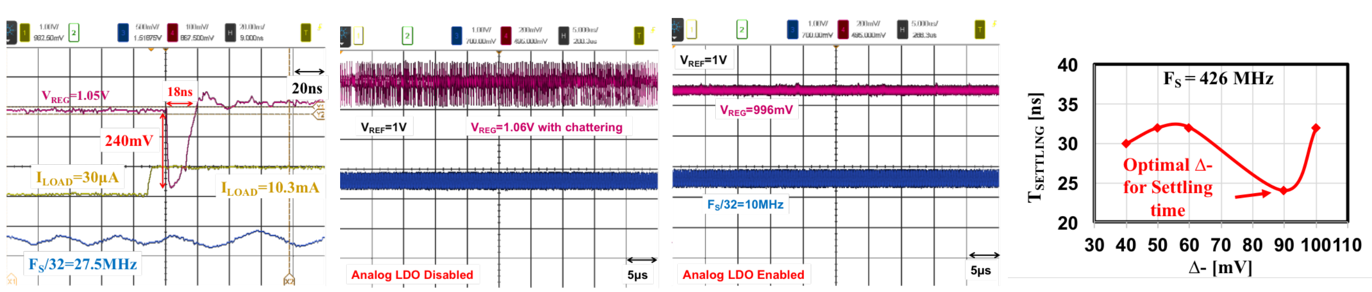
Large Signal (LS) Controller: A synchronous all-digital LDO [3] with 16 output power transistors is implemented to provide a fast LS response. It comprises of four stages: (1) detection stage to determine the magnitude of the voltage error, (2) comparison stage to determine the sign of the voltage error, (3) control stage, and (4) actuator stage. Stage (1) consists of two strongARM latch based clocked comparators. They are used to compare V_{REG} with $V_{REF}-\Delta_-$ and $V_{REF}+\Delta_+$ to establish if $V_{REF}-V_{REG}>|\Delta|$. The comparators are designed to operate up to 1 GHz. If V_{REG} is found to be $<V_{REF}-\Delta_-$ or $>V_{REF}+\Delta_+$, i.e., out of the dead-zone, the clock signal is un-gated to the following comparison stage. The comparison stage (Stage 2) consists of a single strongARM latch based clocked comparator. It is only operational if the clock is available to it from the preceding detection stage. Once on, it compares V_{REG} with V_{REF}. The control stage (Stage 3) consists of a 16-bit bidirectional shift register. If $V_{REG}<V_{REF}$, the shift register passes a '0' to turn on a power transistor and if $V_{REG}>V_{REF}$ then it passes a '1' to turn off a power transistor, in the final actuator stage. The comparison stage operates at the positive clock edge, whereas, the control stages uses the negative clock edge for its operation. This ***dual edge triggering*** allows a lower control signal latency. The final actuator stage (Stage 4) consists of an array of 16 power transistors. They are designed to provide a maximum current (I_{LOAD}) of 12 mA consuming a total area of 27.68 μm^2. The clock for the LS controller is generated through a 5 stage current starved inverter based voltage controlled oscillator. The voltage control is available externally on a pad. The oscillator frequency can be tuned up to 1 GHz. A detailed circuit implementation of the LS controller is shown in Fig. 4.

Small Signal (SS) Regulator: An OPD analog LDO is designed to provide high gain and bandwidth for SS regulation. Since the requirement on the SS regulator is only 10-20% of the maximum load current, the proposed LDO is designed to deliver 40 µA to 2.5 mA without the use of any internal capacitors to achieve stable operation. This is achieved by creating two replicas, each capable of providing providing up to 1.25 mA current while consuming less than 82 µA quiescent current. The first stage of the OPD analog LDO comprises of a self biased transconductance (gm) stage which uses a differential pair with diode connected transistors at the input, as shown in Fig. 5a. To make the output node pole dominant, all the internal poles of the LDO need to be at frequencies at least 10X higher than the output pole. This is achieved by employing two separate techniques

1) Using smaller size of the power transistor through hybrid topology.

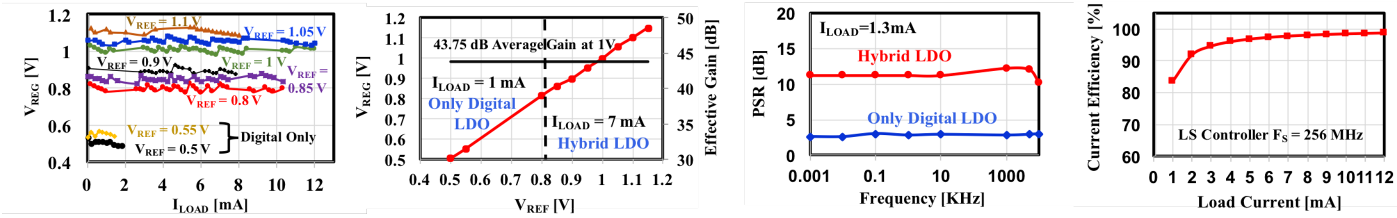
2) Putting in a shunt buffer between the first stage and the power transistor to further push the pole at the gate of the power transistor to a higher frequency.

An adaptive shunt buffer stage is inserted between the power transistor and the gm stage [9]. If the first stage is directly connected to the power transistor, the impedance at the power transistor gate is not small enough to guarantee stability with the output capacitance in sub nF range. Therefore, the shunt buffer stage is used to divide this pole (second dominant) in to two higher frequency poles ($P_2 \approx 1/2\pi R_{OUT,OTA}C_{GS,M11}$ and $P_3 \approx 1/2\pi R_{OUT,BUFF}C_{GS,MPA} \approx (gm_{11}(1+gm_{13})+gm_{12})/2\pi C_{GS,MPA}$). P_2 is pushed to a higher frequency as the gate capacitance



(a) (b) (c) (d)

Fig. 6 . Measured response at V_{IN}=1.2V. (a) Transient response. (b) Steady state response with SS regulator disabled. (c) Steady state response with SS regulator enabled. (d) Optimal Δ_- at iso-F_S.



(a) (b) (c) (d)

Fig. 7. Measurement results with V_{IN}=1.2V (for hybrid), V_{IN}=0.6V (digital only). (a) Load regulation. (b) Line regulation. (c) Power suply noise rejection. (d) Current efficiency (including clock generation and distribution).

offered by M_{11} is very small compared to that of M_{PA}. P_3 is pushed to a higher frequency as the resistance at the gate of M_{PA} decreases due to the shunt feedback implemented through transistors M_{11}-M_{13}. M_{11} samples the voltage at the gate of the power MOS and uses M_{13} to adjust the current to complete the shunt feedback loop. The gain of the loop dictates the decrease in the resistance and thus the location of P_3. Worst stability condition for the SS regulator occurs at maximum load current, as the dominant output pole is at its highest possible frequency. Maintaining a high phase margin (PM) requires the shunt feedback loop to be effective when the voltage at the gate of M_{PA} has decreased to provide maximum load current. This is ensured by increasing the biasing current flowing through the diode connected transistor M_{12}. A simulated bode plot near I_{MAX}, shown in Fig. 5b, highlights the achieved high PM. Scan programmable synthetic load is developed to mimic the operation of digital loads.

V. Results and Measurements

Chip micrograph of the presented hybrid LDO is shown in Fig. 5c. The LDO runs from a V_{IN} of 1.1 to 1.2 V with a dropout (V_{DO})=100-300mV and provides I_{LOAD}=12mA at a nominal V_{DO}=100mV. For V_{IN}=0.6V (NTV mode), the LDO is reconfigured to operate in a fully digital mode. It regulates for a V_{DO}=50mV and provides I_{LOAD}=2mA at V_{REG}=0.5V. Fig. 6a shows the scope capture of fast transient response. A T_{RISE}=18ns and $T_{SETTLING}$=32ns (<2% of V_{REG}) is achieved for a load step of 30µA to 10.3mA at V_{REG}=1.05V from V_{IN}=1.2V. Similarly, fig. 6b shows the chattering (unstable behavior) if SS regulator is disabled as compared to the stable response when it is enabled as shown in fig. 6c. It shows the perfect marriage of a quasi-stable LS digital controller with a damped SS analog controller. A higher F_S ensures a faster T_{RISE} and $T_{SETTLING}$ with a decrease in V_{DROOP} to large load steps. To ensure stable operation, Δ_-=90mV below V_{REF} and Δ_+=20mV above V_{REF} is selected to ensure optimal settling behavior across the complete operational range (Fig. 6d). Extensive load regulation measurements (Fig. 7a) are performed across the complete operational range. The worst case measurement showed 2.67mV/mA load regulation. It can be improved by increasing the SS regulator gain at maximum load current. The hybrid topology exhibits high line regulation (on average < 5mV error) as shown by the linearity of graph in Fig. 7b. As opposed to purely digital LDO topologies, which fail to provide high power supply noise rejection (PSR), the presented hybrid topology shows an average of 12dB PSR from 1 Hz to 10 MHz. As shown in Fig. 7c, the high bandwidth of the PSR graph (and the absence of PSR peaking which is typical of IPD LDOs due to degradation of loop gain) also demonstrates the output pole dominant behavior of the designed SS regulator. A peak current efficiency of 98.64% is measured (Fig. 7d), which includes all the dynamic power consumed in clock generation and distribution. Competitive performance is achieved when compared with state of the art as summarized in Table. II.

Table II. COMPARISON TABLE

	This Work	[1]	[2]	[3]	[4]
Type	LDO	LDO	LDO	LDO	LDO
Technology	130 nm	45 nm SOI	65 nm	130 nm	65 nm
LDO Type	Digital + Analog	Multiloop	Analog	Digital	Digital
Control methodology	SMC	Linear	Linear	Adaptive	Linear
Control Reconfigurability	Yes	No	No	Yes	No
V_{IN} (V)	0.6, 1.1-1.2	1.179 - 1.625	1.15	0.5 - 1.2	0.6 - 1.0
V_{OUT} (V)	0.5 - 0.55, 0.8 - 1.1	0.9 - 1.1	1	0.45 - 1.14	0.55 - 0.95
Load Current: I_{MAX} (mA)	12	42	10	4.6	500
Load Regulation (mV/mA)	< 2.67	9.8	0.15 - 0.2	< 10	0.25
Controller Current: I_{CTL}(uA)	163.2	9450	50	24 - 221	300
Total Capacitance (nF)	0.5	1.46	0.14	1	1.5
Active Area (mm^2)	0.0818	0.075	0.0234	0.114	0.158
Peak Current Efficiency (%)	98.64	77.50	99.50	98.30	99.99
Droop (mV) @ Load Step (mA)	240 @ 10.3	7.6 @ 4.5	43 @ 10	40 @ 0.7	35 @ 100
Droop recovery time (ns)	18	NA	100	300	40
FOM1 (ns/mA)	1.747	NA	10	428.5	0.4
FOM2 (ps)	244.8	62.4	3.01	0.0765*	1.6

FOM1= Droop recovery time / Load Step; FOM2= (Transient Time) * I_{CTL}/ I_{MAX}

NA - Insufficient data; * Normalized to technology node

Conclusion

A hybrid LDO based on SMC designed in 130nm CMOS process features both digital and analog loops. The design is tailored to meet PoL regulation in digital load circuits with wide work-load dynamics. Measurements show peak response time of 18 ns for large load transients, low voltage operation programmability and a peak current efficiency of 98.64%.

References

[1] Bulzacchelli, J. F., et al. "Dual-loop system of distributed microregulators with high DC accuracy, load response time below 500 ps, and 85-mV dropout voltage." *IEEE JSSC, vol.* 47, no. 4 pp. 863-874, Apr. 2012.

[2] Lu, Y, et al. "A 0.65 ns-response-time 3.01 ps FOM fully-integrated low-dropout regulator with full-spectrum power-supply-rejection for wideband communication systems." *in IEEE ISSCC, 2014.*

[3] Nasir, S. B., et al. "A 130nm Fully-Digital Low-dropout Regulator with Adaptive Control and Reduced Dynamic Stability for Ultra-wide Dynamic Range." *in IEEE ISSCC, 2015.*

[4] Yang, F., et al. "A 0.6–1V input capacitor-less asynchronous digital LDO with fast transient response achieving 9.5 b over 500mA loading range in 65-nm CMOS." *in IEEE ESSCIRC*, 2015.

[5] Gangopadhyay, S., et al. "A 32 nm Embedded, Fully-Digital, Phase-Locked Low Dropout Regulator for Fine Grained Power Management in Digital Circuits," in *IEEE JSSC*, vol. 49, no. 11, pp. 2684-2693, Nov. 2014.

[6] Gangopadhyay, S., et al. "UVFR: A Unified Voltage and Frequency Regulator with 500MHz/0.84V to 100KHz/0.27V Operating Range, 99.4% Current Efficiency and 27% Supply Guardband Reduction" in *IEEE ESSCIRC*, 2016.

[7] Hazucha, P, et al. "Area-efficient linear regulator with ultra-fast load regulation." *IEEE JSSC, vol.* 40, no. 4 pp. 933-940, 2005.

[8] Lee, Yong-Jin, et al. "A 200mA digital low-drop-out regulator with coarse-fine dual loop in mobile application processors." *in IEEE ISSCC, 2016.*

[9] Al-Shyoukh, M., et al. "A transient-enhanced low-quiescent current low-dropout regulator with buffer impedance attenuation." *IEEE JSSC, vol.* 42, no. 8 pp. 1732-1742, 2007.