UVFR: A Unified Voltage and Frequency Regulator with 500MHz/0.84V to 100KHz/0.27V Operating Range, 99.4% Current Efficiency and 27% Supply Guardband Reduction

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***Abstract*—A fully-digital, single-loop Unified Voltage and Frequency Regulator (UVFR) is designed in 130nm CMOS to provide the correct supply to digital loads to meet a timing criteria. Simultaneously a Tunable Replica Circuit (TRC) based local oscillator is generated from the regulated supply and clocks the load. Measurements show 0.84V to 0.27V range of operation, and 27% supply guardband reduction at iso-performance through adaptation and resiliency which are intrinsic to the control loop.**

***Keywords*—LDO, clocking, adaptation, resiliency, DVFS**

I. Introduction

Fine-grained Dynamic Voltage and Frequency Scaling (DVFS) continue to pose significant challenges to power delivery, voltage regulation and clocking. Compact, power-efficient LDOs capable of supplying large load transients are being actively researched [1-4]. Similarly, advanced PLL [5] and clock distribution [6] techniques that respond to supply voltage droops have been proposed. But their effectiveness is limited. Droop sensitivity in [5] is limited by the PLL loop BW. [6] requires complex auto-tuning or calibration, high-overhead clock buffers and finely-controlled clock gating. Conventional systems are limited by the fact that voltage and frequency are generated by separate control loops. Motivated by the observation that the main objective of supply voltage regulation in digital systems is meeting timing, we present a Unified Voltage Frequency Regulator (UVFR) that sets the supply voltage based on system timing properties, and minimizes supply noise margins by temporarily modulating the clock frequency. Synthesized from all-digital cells, which generates and co-regulates a local clock and the local supply voltage simultaneously, the UVFR powers a digital load circuit block embedded in a multi-domain SoC. Here a frequency-only reference is provided (F_{REF}) from a shared PLL. The regulated supply (V_{REG}) is locally generated at one point in the loop and a local VCO clock (can be divided by N) which is locked to the reference (F_{LOC}=NF_{REF}) is generated at another point of the same loop (Fig. 1), providing a tightly coupled F_{LOC}-V_{REG} pair and the DVFS state is only defined uniquely by performance (F_{REF} which is equal to F_{LOC}).

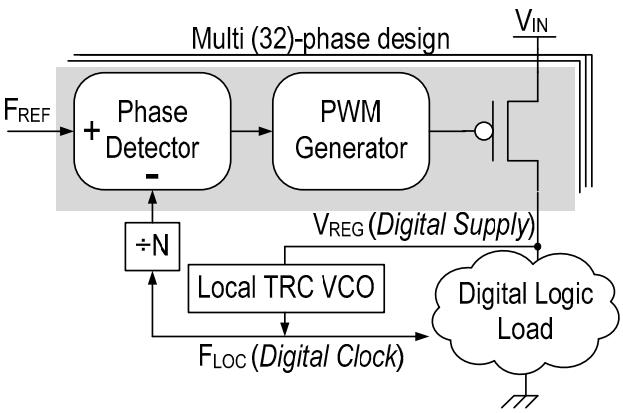


Fig 1: Unified Voltage Frequency Regulator (UVFR) Architecture

II. UVFR Design and Principle of Operation

UVFR system utilizes two clocks F_{REF}, the reference frequency generated from a shared PLL and F_{LOC} generated from a local VCO (LVCO) that is powered by V_{REG}. Fig. 2 illustrates the circuit implementation with N=1. The reference clock and the LVCO outputs are used to clock a 16-bit Johnson Counter (JC) with overrun protection [8], PWM generation and embedded output drivers.

The outputs of the different JC stages (R_i for reference clock and L_i for local clock) form multi-phase and 16x subsampled versions of the reference clock and the LVCO clock. Another 16-bit JC triggered by the negative clock edges provide further multi-phase capabilities. At steady-state condition, the phase difference between F_{REF} and F_{LOC} locks to a constant value and turns the power P-MOS 'on' for the exact duration of time that the load current demands to keep V_{REG} constant. The phase locking occurs at each stage of the JC and the total current provided by all the PMOS devices in a time interleaved manner enables voltage regulation. If a load transient causes the V_{REG} to decrease from its steady state value, then the LVCO responds by slowing down F_{LOC} and stretching the pulse at L_i. This perturbs the phase locking and creates additional phase difference allowing the pull up devices to supply higher current until re-locking and regulation are again achieved. Similarly, if the V_{REG} increases from its steady state value F_{LOC} speeds up, which reduces the phase difference and the loop goes out of lock. This in turn reduces the supply of current by the pull-up devices and ultimately reduces V_{REG} until re-locking is achieved. The process locks F_{REF} to F_{LOC} and a multi-phase design enables a ripple-free V_{REG}.

The overrun protection (OP) circuit removes any phase aliasing in the XOR based phase detector (PD) (Fig. 3a), and its circuit implementation (Fig. 3b) consists of the logic that (a) holds the value of R_i if L_i=R_i and propagates the previous

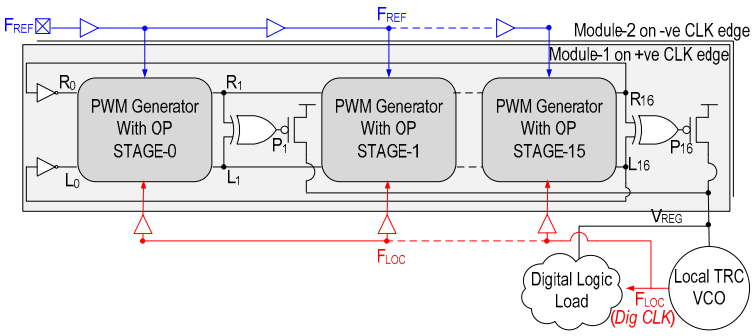


Fig 2: Johnson Counter based multi-phase Unified Voltage Frequency Co-regulator (Here N=1)

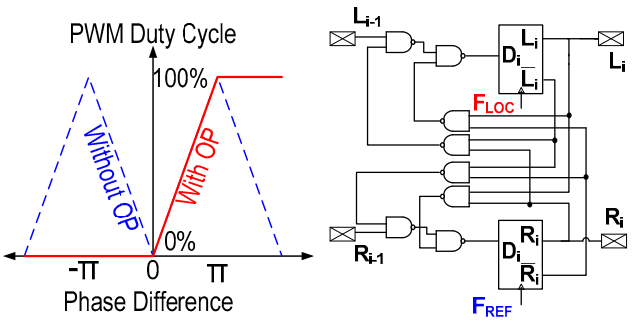


Fig 3: (a) Overrun Protection (OP) prevents aliasing in large phase errors (b) OP circuit implementation

stage value (R_{i-1}) to R_i if $L_i \neq R_i$ and (b) holds the value of L_i if $L_i \neq R_i$ and propagates the previous stage value (L_{i-1}) to L_i if $L_i = R_i$. The OP block is needed to remove the locking range limitation imposed by the XOR gate based phase detector. Instead it is able to lock the loop and operate till the maximum current limitation of the power devices. During a large load transient, when F_{LOC} slows down with respect to F_{REF}, the phase difference F_{LOC} and F_{REF} saturates to π. This implies 100% duty cycle for the pull-up devices i.e. the devices remain on throughout the cycle and provide the maximum load current possible. On the other extreme if the F_{LOC} compared to F_{REF} is high due to either a change in F_{REF} or a large negative load step, then the phase difference approaches 0. This implies that the pull devices are turned off until the output voltage decreases to restore the locking between F_{REF} and F_{LOC}. It is interesting to note that the JC computes phase differences in parallel. By virtue of the fact that at any instance, at least one stage of the JC is operating on an edge, any perturbation from the steady-state condition is immediately identified and corrective action is taken.

The UVFR is designed to drive digital load circuits. In the current design, the digital load consists of a pipeline state (of random logic) with error-detection capability (Fig. 4) where a positive latch and a positive edge triggered flip-flop sample

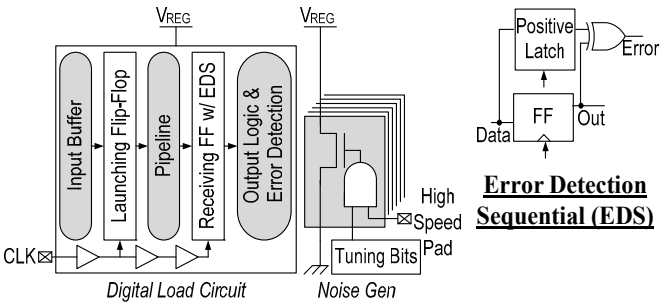


Fig 4: Digital Logic Load with (1) pipeline with EDS and (2) programmable DC load and (3) programmable noise generator

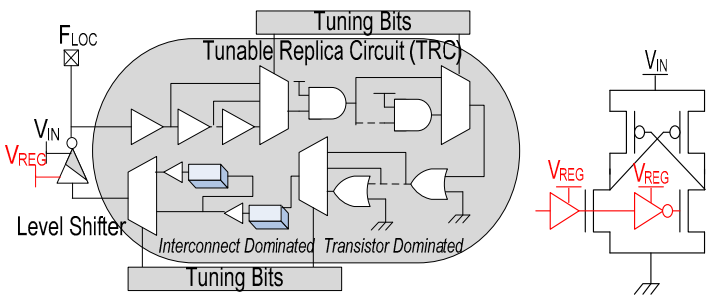


Fig 5: (a) TRC based oscillator acts as VCO (b) level shifter schematic

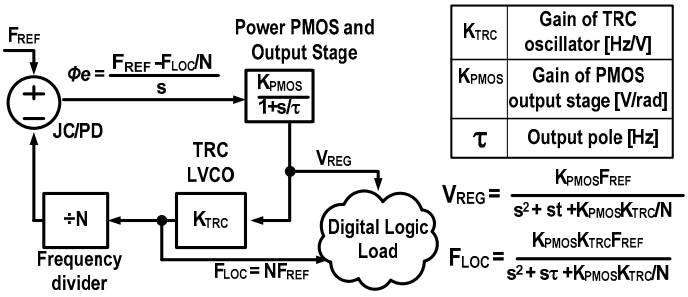
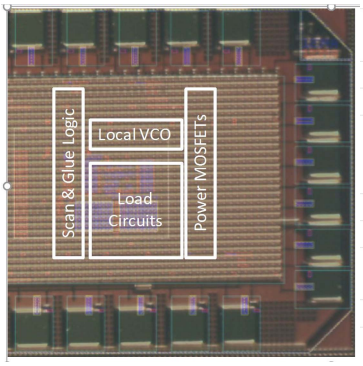


Fig 6: Small signal s-domain model of the UVFR control loop

the same data and produce an error signal if they are unequal – which signifies a delay induced error. The error detection window is equal to the high phase of the clock and for droops of up to 35% we can correctly capture any pipeline error. Scan programmable DC load circuits and high-speed noise generation circuits are integrated to mimic a large dynamic load range, and abrupt load steps characteristic of power gating/un-gating or power state transitions in realistic load conditions. Capability is provided through high speed pads to excite load transients as well as observe F_{REF}, F_{LOC}, error signals from the pipeline output and the output voltage node, V_{REG}. The LVCO consists of a scan programmable non-inverting Tunable Replica Circuit (TRC) which is calibrated to mimic half the critical path delay and consists of both transistor-dominated and interconnect-dominated segments (Fig. 5(a)). It is half because $1/F_{REF}$ should equal to twice the TRC path delay. An inverting level shifter performs the following functions: (1) It acts as TRC timing guard-band of less than 5%. (2) It closes the TRC loop to form the LVCO and (3) it feeds the JC. The schematic diagram for the level shifter has been provided in the Fig. 5(b). At steady state, V_{REG} is at the correct voltage such that the TRC based VCO locks its frequency to F_{REF}. Consequently, V_{REG} is also the correct voltage to enable the critical path of the pipeline circuit to meet the timing requirement ($1/F_{REF}$). The digital load is clocked by LVCO. Hence, any voltage droop (overshoot) at V_{REG} leads to LVCO slowing down (speeding up) proportional to the critical path thereby preventing delay errors in the pipeline. This leads to a larger (smaller) phase difference between F_{REF} and F_{LOC} which in turn increases (decreases) the duty cycle of power MOSFETs [8]. This brings V_{REG} back to regulation and F_{LOC} back to F_{REF} simultaneously.

To understand the system dynamics, we linearize the loop and Fig. 6 shows the small signal s-domain model for the UVFR control. It is a second order system where V_{REG} and F_{LOC} are tightly coupled to each other. It can be seen from the model



Process	GF 130 nm 8M-CMOS
Package	QFN
Active Area	0.0204mm2
Total Area Including peripherals	0.11 mm2
Input VDD	0.6V-1V
Output VREG	0.27V-0.84V
Reference Frequency	100KHz-500MHz
Load Current	100uA-6mA

Chip Characteristics

Fig 7: Chip micrograph and characteristics

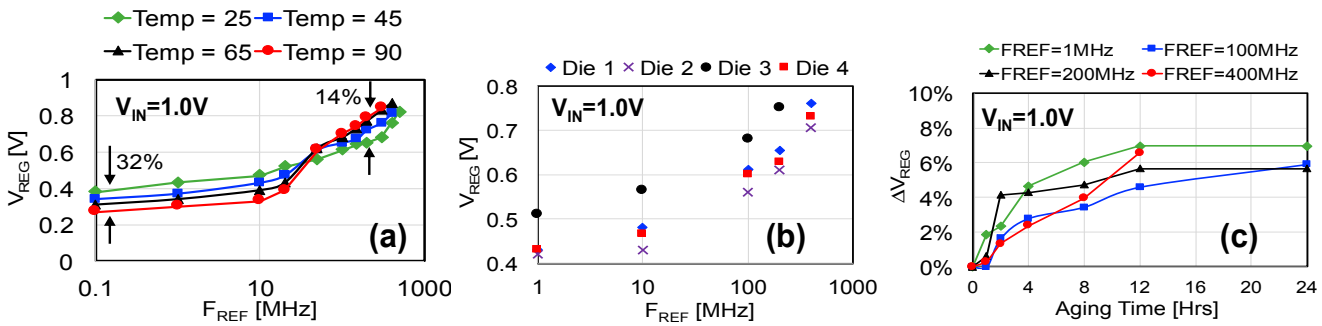


Fig 8: Measured results show V_{REG} adapting with (a) Temp, (b) process variation and (c) aging to maintain frequency lock. The process V_{TH} = 350mV and UVFR operates from 0.84V to 0.27V NTV (near threshold voltage).

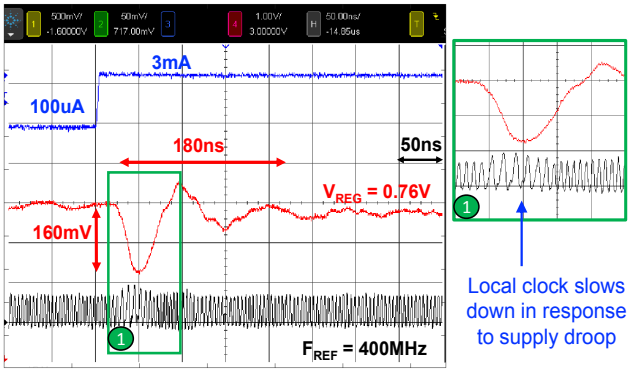


Fig 9: Measured scope capture showing full load step and local clock adapting to V_{REG} changes

that the F_{LOC} is linearly coupled to V_{REG}. However, it should be noted that the linearity is assumed for the purpose of the small signal model only. In reality, even if F_{LOC} changes non-linearly with V_{REG} (which is typical for large droops), as long as the the sensitivity of the TRC and the critical path to the supply voltage are similar, the system will not let the pipeline incur a delay error. Further, any jitter on F_{LOC} is perfectly correlated to V_{REG}, (which dominates over any random component) and creates a V_{REG}-F_{LOC} pair. The design is fabricated in GF 130nm 8-M CMOS process and the UVFR occupies an active area of 0.0204mm^2 as shown in Fig. 7. The total silicon area which includes active devices, local VCO, load circuit and scan logic is 0.11 mm^2. The test-interface is a QFN package. UVFR has low calibration overhead. Instead of calibrating the supply voltage corresponding to a frequency (as in conventional DVFS), we calibrate the TRC setting corresponding to a reference frequency in UVFR at no extra test-time. Additionally, most current designs already employ TRC as run-time monitors, which make the design and test overhead negligible.

III. Measurement Results

UVFR allows V_{REG} to autonomously adapt to PVT while the LVCO maintains frequency locking to the reference.

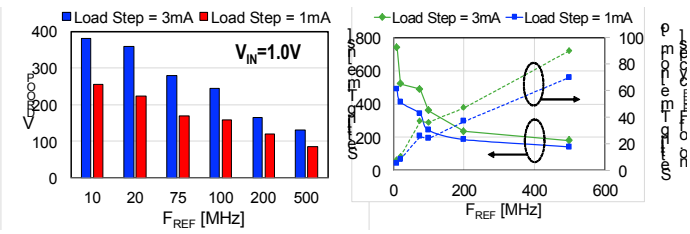


Fig 10: Measured (a) voltage droop and (b) settling time for varying F_{REF}.

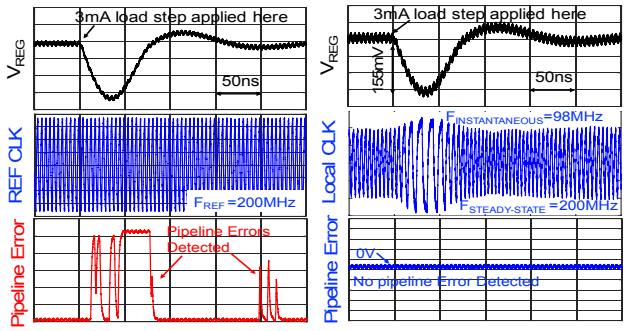


Fig 11: Measured scope data on high-speed active probe shows UVFR enables error-free operation even under large droops

Measurements in Fig. 8 illustrate how V_{REG} automatically changes with F_{REF} all the way to the Near Threshold Voltage (NTV) operation. At F_{REF}=100KHz and T=90C, the loop maintains regulation with V_{REG}=270mV which is below process V_T (linear V_T=300mV). At F_{REF}=500MHz and T=25C, the loop locks with V_{REG}=0.84V. Further the loop can track temperature (Fig. 8a), process (Fig. 8b) and aging (Fig. 8c) providing just enough V_{REG} to maintain the frequency lock and eliminating voltage guard-bands (measured: 14-32% for temperature, 30% for process, 6-7% for aging). Oscilloscope capture for a 3mA load step at F_{REF}=400MHz (Fig. 9) shows 180ns droop recovery time and the corresponding LVCO slow-down. As F_{REF} increases (system goes from low power to high performance mode) the voltage droop decreases (Fig. 10a) and the settling time improves (Fig. 10b). We note that at lower F_{REF}, the system settles in a smaller number of clock cycles and at F_{REF} =500MHz, the system settles down in 91 clock cycles. However, unlike in conventional designs where the pipeline has to wait for the voltage regulator and the PLL to both settle before operation can be restarted, the UVFR, by virtue of the coupled VREF-F_{LOC} loop allows error-free operation even during load transients and we observe (from a wide array of experiments across PVT and load ramp rates) no pipeline error. Measurements from oscilloscope captured data in Fig. 11 illustrate the ability of the UVFR scheme to provide resiliency to delay errors. As the V_{REG} droops (under load step), a baseline design (where the digital load is clocked by F_{REF}) shows characteristic error profile, whereas the UVFR continues to operate without any pipeline error, demonstrating perfect compensation between clock and data and works across all frequency and voltage ranges as long as the TRC is well calibrated.

Fig. 12(a) shows ~2mV/mA of load regulation for different F_{REF}-V_{REG} combinations. Fig. 12(b) shows ~10mV/V line regulation with corresponding frequency locking (measured as

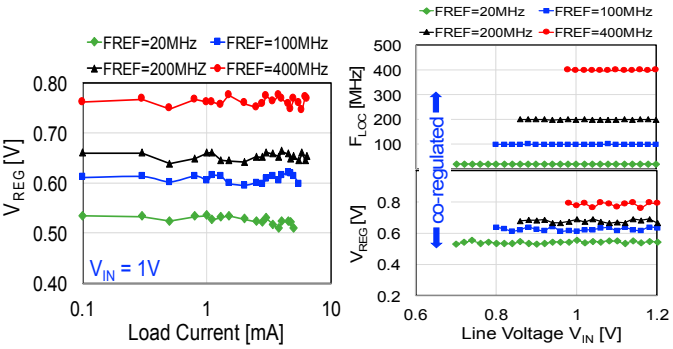


Fig 12: (a) Measured load regulation (b) Measured line regulation

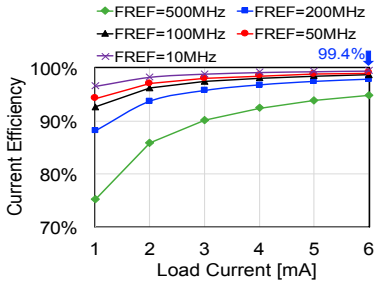


Fig 13: Measured data shows high current efficiency (>99%) for majority of the operating reference frequencies.

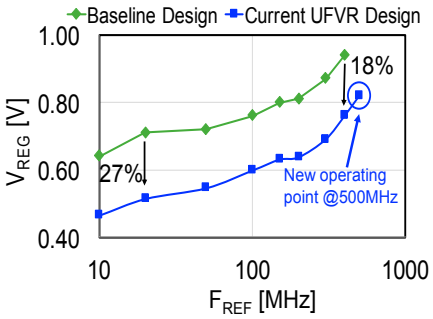


Fig 14: Measured performance and voltage regulation shows 18%-27% supply reduction for iso-frequency

an average over 1000 cycles) and the concept of F_{REF}-V_{REG} co-regulation. It should be noted that during these measurements, the digital load circuit was continuously clocked. In Fig. 13 current efficiency vs. load current has been shown across a range of reference frequencies from 10 to 500 MHz. The UVFR macro consumes 36µA(@F_{REF}=100KHz) to 330µA(@F_{REF}=500MHz) (V_{IN}=1V) and shows a peak current efficiency of 99.4%. Fig. 14 shows the measured supply-performance trade-off between the baseline design and the UVFR design. Owing to a smaller guard-band UVFR enables 18-27% reduction of V_{REG} at iso-F_{REF}. Only the droop induced guard-band is considered here, as PVT sensors can potentially reduce voltage guard-bands in baseline designs as well.

Table 1 shows comparison of the LDO characteristics with other published results and show competitive FOMs. Table 2 compares UVFR with supply aware clocking techniques and this unique single-loop 'clock and supply regulation' provides inherent adaptation and resiliency resulting with significant guard-band reduction.

IV. Conclusions

A single-loop UVFR in 130nm CMOS has been presented. Measured data across a wide range of voltage and current inputs reveals peak current efficiency of 99.4% and 27% supply reduction at iso-performance through adaptation and resiliency which are intrinsic to the control loop.

	This Work	[1]	[2]	[3]	[4]
Type	LDO+Clock	LDO	LDO	LDO	LDO
Technology	130 nm	40 nm	130 nm	45 nm SOI	65 nm
LDO Type	digital	Digital	Digital	Multiloop	Digital
Control methodology	Co-regulation	Linear	Adaptive	Linear	Linear
V_{IN} (V)	0.6-1V	0.6	0.5 - 1.2	1.179 - 1.625	0.6 - 1.0
V_{OUT} (V)	0.38-0.81V	0.4	0.45 - 1.14	0.9 - 1.1	0.55 - 0.95
Load Current: I_{max} (mA)	6	200	4.6	42	500
Load Regulation (mV/mA)	< 1.8	0.05	< 10	9.8	0.25
Controller Current: I_{CTL} (uA)	36-330	25.1	24 - 221	9450	300
Total Capacitance (nF)	0.2	Cap-free	1	1.46	1.5
Active Area (mm^2)	0.0204	0.0375	0.114	0.075	0.158
Peak Current Efficiency (%)	99.40	99.99	98.30	77.50	99.99
Droop (mV) @ Load Step (mA)	163@3	NA	40 @ 0.7	7.6 @ 4.5	35 @ 100
Droop recovery time (ns)	200	NA	300	NA	40
FOM1 (ns/mA)	0.32	NA	428.5	NA	0.4
FOM2 (ps)	666	NA	0.0765*	62.4	1.6

FOM1= Droop recovery time / Load Step; FOM2= (Transient Time) * I_{CTL}/ I_{MAX}
NA - Insufficient data; * Normalized to technology node

Table 1: Comparison with LDOs for voltage regulation

	Type	Tech	Technique	Calibration Requirement	Freq Adaptation Range	Improvement
This Work	LDO + Clock	130nm	Co-regulation	limited (TRC calibration)	DC to any Freq	27%(voltage)
[5]	PLL Control	45nm	compensation through DCO	Extensive	outside PLL BW	5% (performance)
[6]	Clock Distribution	16nm	Adaptation to droops in clock tree	Auto	limited by latency of CLK distribution	NA

Table 2: Comparison with voltage aware clocking techniques

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