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Characterization and Modeling of 22nm FDSOI Cryogenic RF CMOS

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***Abstract*— Analog and RF mixed-signal cryogenic-CMOS circuits with ultra-high gain-bandwidth product can address a range of applications such as interface circuits between Superconducting Single-flux Quantum (SFQ) logic and cryo-DRAM memory, circuits for sensing and controlling qubits faster than their de-coherence time for at-scale quantum processor. In this work, we evaluate RF performance of 18nm gate length (L_G) FDSOI NMOS and PMOS from 300K to 5.5K operating temperature. We experimentally demonstrate extrapolated peak unity current-gain cutoff frequency (f_T) of 495/337 GHz (1.35x /1.25x gain over 300K) and peak maximum oscillation frequency (f_{MAX}) of 497/372 GHz (1.3x gain) for NMOS/PMOS, respectively, at 5.5 K. A small-signal equivalent model is developed to enable design-space exploration of RF circuits at cryogenic temperature and identify the temperature-dependent and temperature-invariant components of the extrinsic and the intrinsic FET. Finally, performance benchmarking reveals that 22nm FDSOI cryogenic RF CMOS provides a viable option for achieving superior analog performance with giga-scale transistor integration density.**

***Index Terms*—** *Cryogenic-CMOS, Quantum Processor, 22nm FDSOI Technology, Small-Signal-Equivalent Circuit Model, Cut-off frequency (f_T), Maximum Oscillation frequency (f_{MAX})*

I. INTRODUCTION

CRYOGENIC superconducting (SC) digital processors operating at 4K, employing Josephson junctions for single flux quantum (SFQ) logic, offer the promise of greatly reduced operating power for high-performance cloud compute systems due to the exceptionally low energy per operation of SFQ circuits [1]. This allows a significant reduction in overall energy delay product and hence has led to renewed interest in superconducting computing with SFQ. It is equally important to complement superconducting logic technologies with a compatible high-bandwidth, low latency memory technology co-located in the same 4K temperature plane. For instance, operation of 1.3 GHz embedded DRAM macro with 2T-Gain-Cell was demonstrated at 4K as an option for ultra-high density cryo-memory sub-system for SFQ logic processors [2]. Integration of cryogenic-DRAM in the same thermal plane as the JJ superconducting logic shortens the interconnect length and improves data access latency. Reduced sub-threshold leakage through the DRAM access transistor at cryogenic temperature was harnessed to enable 10^6x higher retention time and consequently lower refresh power [2]. Memory capacity of Cryogenic-DRAM can further be increased by designing the DRAM memory cell at denser CMOS nodes. Interfacing cryogenic DRAM with superconducting logic still remains a technology challenge. For instance, SFQ logic operates with 2 mV amplitude pulses with picosecond duration which make implementation of input and output circuits challenging. Also, JJs by themselves cannot directly drive bit/wordline or CMOS sense amplifiers in DRAM arrays, which operate at 0.8V to 1V supply. In this context, multi-stage signal booster and level translator circuits with high gain (400V/V) and GHz bandwidth, are required to interface SC circuits with cryo-DRAM memory. Furthermore, cryogenic-CMOS based analog and mixed signal interface systems has been proposed for control and read out of qubits in a large-scale quantum computer [3]. Placing the cryo-CMOS control electronics in close physical proximity to the quantum processor can provide significant benefits in-terms of system scalability and low latency [4]. As the cryogenic qubit controller requires generation and acquisition of GHz range signals with low power dissipation and high immunity to noise [5], design-space exploration of cryogenic RF circuits is required to ensure strict power budgets along with superior

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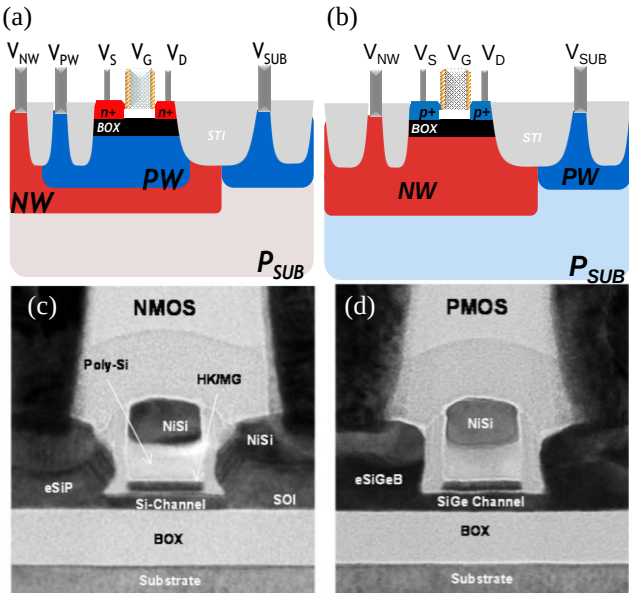

Fig 1. Schematic of device structure and xTEM image of regular-well 22nm FDSOI for (a, c) Si nFET and (b, d) SiGe pFET respectively, as shown in [6]

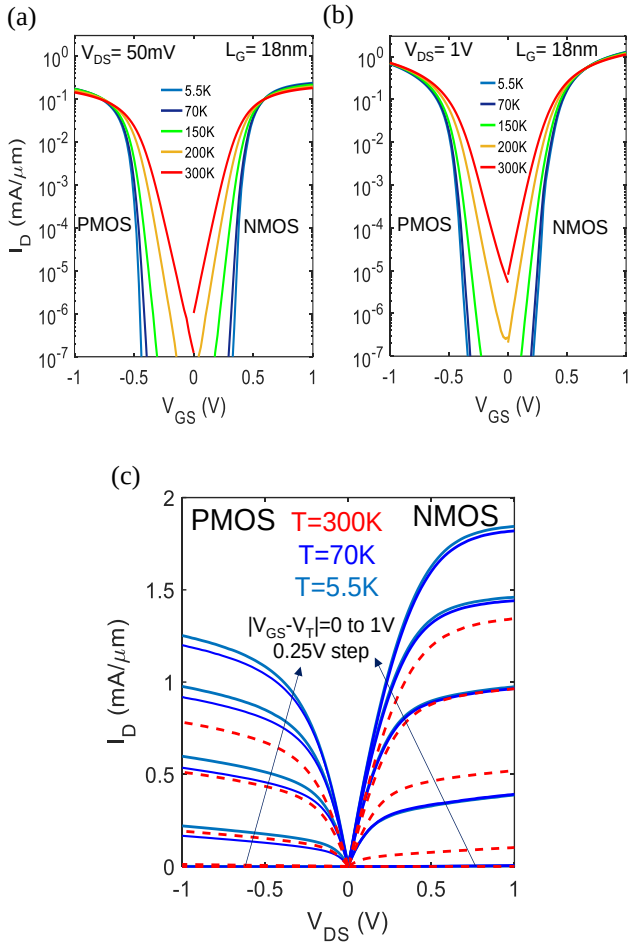

Fig. 2. Transfer characteristic of 22nm FDSOI nFET and pFET (L_G=18nm) from 300K to 5.5K in (a) linear (V_{DS}=|50mV|) and (b) saturation (V_{DS}=|1V|) region, (c) Output characteristic of nFET and pFET (L_G=18nm) at 300K, 70K and 5.5K

analog and RF performance.

The ultra-thin body and buried-oxide (UTBB) fully-depleted silicon-on-insulator (FDSOI) CMOS platform is a potential platform for both of the above-mentioned cryogenic RF application, due to high transistor density, low power dissipation, reduced parasitic and optimized RF performance [6], [7]. Commercially available FDSOI CMOS technologies (22nm, 28nm node) has been investigated in detail down to 4.2K, along with self-heating effects [8] and device variability [9]. However, these studies mainly evaluated the temperature dependence of MOSFET DC parameters, like threshold-voltage, sub-threshold swing, transconductance and drive-current. RF performance of both FDSOI NMOS and PMOS has not been yet studied in detail and quantified at deep cryogenic temperature [10]. In addition, small-signal circuit models for Cryogenic FDSOI is also essential to develop reliable RF circuit design-toolkit, which is still not in existence for 22nm Cryogenic FDSOI technology [11].

This work presents a detailed description and analysis of RF performance gain in 22nm FDSOI technology at cryogenic temperature, as demonstrated in our previous work [12]. In this paper, we investigate RF performance Si NMOS and SiGe PMOS [6] FETs at cryogenic temperature on Globalfoundries 22nm FDX® CMOS platform. Electrical DC and RF characterization of 22nm FDSOI FETs were performed from 300K down to 5.5K. RF Figure-of-Merits (FoMs) such as transistor cut-off frequency (f_T) and maximum oscillation frequency (f_{MAX}) were extracted as a function of Drain current (I_{DS}) bias and operating temperature. Small-signal equivalent circuit of MOSFET [13] was utilized to model the RF response of FDSOI FET from 300 K to 5.5 K. Temperature variation of the small-signal equivalent model parameters was used to identify the temperature dependent and temperature invariant FET parameters that set the limit of Cryogenic RF performance. Finally, performance of 22nm FDSOI FETs at cryogenic temperature is benchmarked against other advanced node Cryogenic CMOS technologies.

II. Device Description and Experimental Details

Commercially available 22-nm FDSOI CMOS technology provides Si channel nFET and SiGe channel (with Ge content around 25%) pFET fabricated with gate-first high-k metal gate process [6]. Fig. 1 shows the device schematic and xTEM of 22nm FDSOI (a, c) nFET and (b, d) pFET respectively. Thickness of the un-doped ultra-thin semiconductor channel is about 6-nm, while the buried oxide is 25 nm thick. Capacitance equivalent thickness (CET) of the high-k gate stack was found to be 1.3 nm. In this work, experimental measurements were

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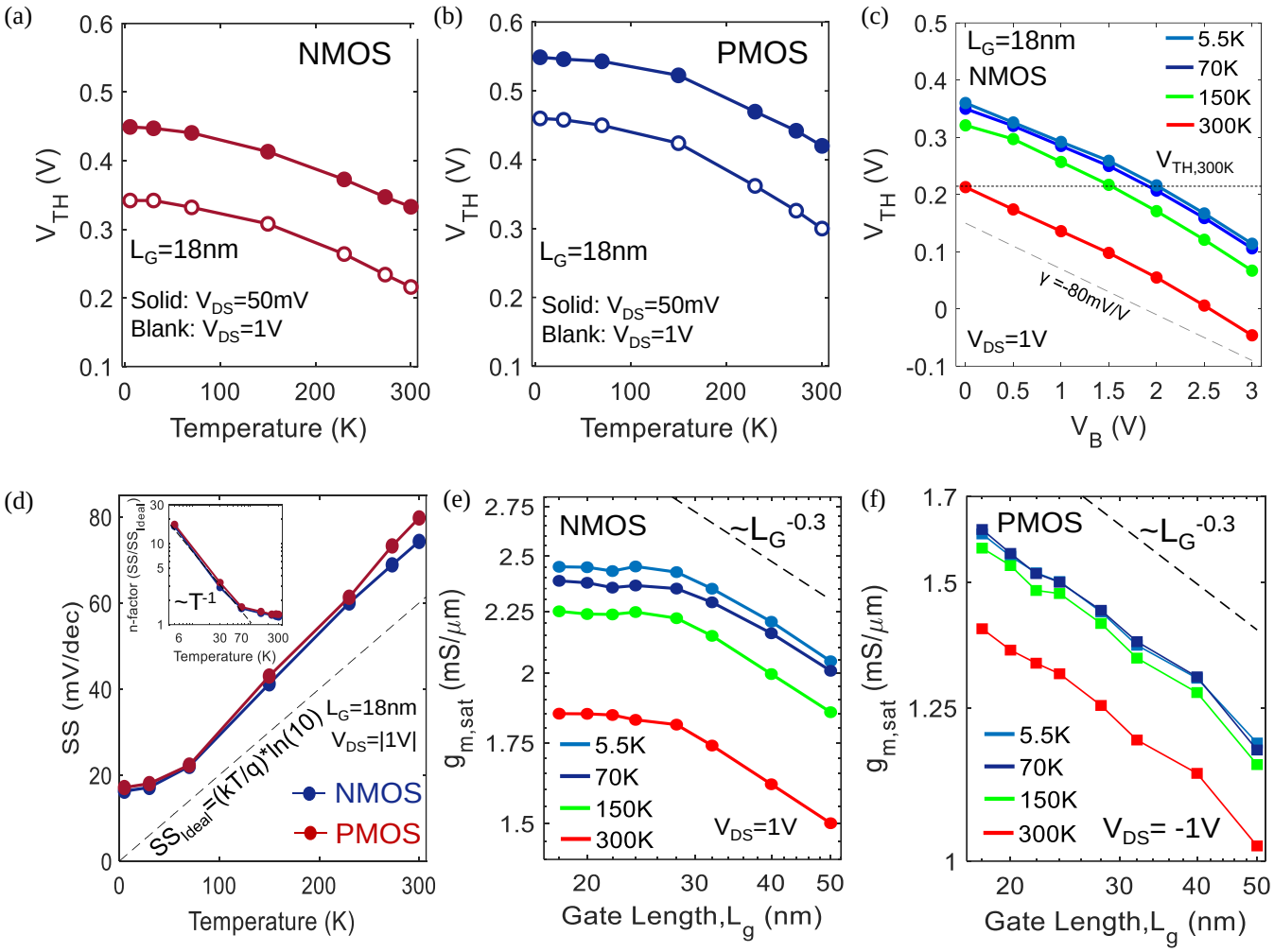

Fig. 3. DC Characterization of Cryogenic FDSOI technology. Threshold voltage shift with temperature at $|V_{DS}|$=50mV and $|V_{DS}|$=1V for (a) nFET and (b) PMOS; (c) 200mV negative shift in V_{TH} can be obtained through back-bias at 5.5K to match the same V_{TH} at 300K. (d) Subthreshold swing (SS) at $|V_{DS}|$=1V for NMOS (blue) and PMOS (red), n-factor (n = SS/SS_{Ideal}) increase sharply with inverse temperature dependence at cryogenic regime (inset), due to high interface trap response capacitance (C_{it}); L_G scaling trend of transconductance ($g_{m,\,Sat}$) at different temperature (300K, 150K, 70K, 5.5K) show constant boost of 33% and 25% for (e) nFET and (f) pFET, respectively

performed down to 5.5 K using Lakeshore CPX-VF cryogenic probe station. Cryogenic DC characterization was performed using a Keithley 4200 SCS parameter analyzer, whereas RF measurement setup consists of GSG (Ground-Signal-Ground) probes with 50 µm pitch and a 8722D vector network analyzer. S-parameters are measured from 300 K to 5.5 K, on 18nm and 28nm LG FETs with 16 gate-fingers of 0.5 µm width each, over 0.5 to 35GHz frequency range, under cold-FET (VDS=0V, |VGS|=0, 0.2V) and saturation (|VDS|=1.0V, |VGS|=0.0 to 1.2V) bias conditions. S-parameters of the on-chip open and short structures are also measured for all temperatures. A two-step de-embedding method using the on-chip Open and Short structures, as described in [14], has been followed to correct for the interconnect-line and access parasitic embedded in the test structure. S-parameters measured on the Open structure were converted to Y parameters (Y_{Open}); this provides the parallel-connected pad and interconnect parasitic. Similarly, the S-parameters of the Short structure were measured and converted to Y parameters (Y_{Short}). The series components of the interconnect parasitic were then obtained from the Open and Short measurements by $Z_{Series} = (Y_{Short} - Y_{Open})^{-1}$, as described in [14]. Finally, the transistor Y-parameters were obtained by measuring the transistor S-parameters, converting them to Z-parameters (Z_{DUT}), and sequentially de-embedding both series and parallel parasitic, using:

$$Y_{Transistor} = ((Z_{DUT}-Z_{Series})^{-1} - Y_{Open}) \quad \ldots (1)$$

where, Z_{DUT} is the Z-parameter representation of the measured device. These de-embedded transistor Y-parameters were then used to extract the RF FoMs of the transistor, such as f_T and f_{MAX}.

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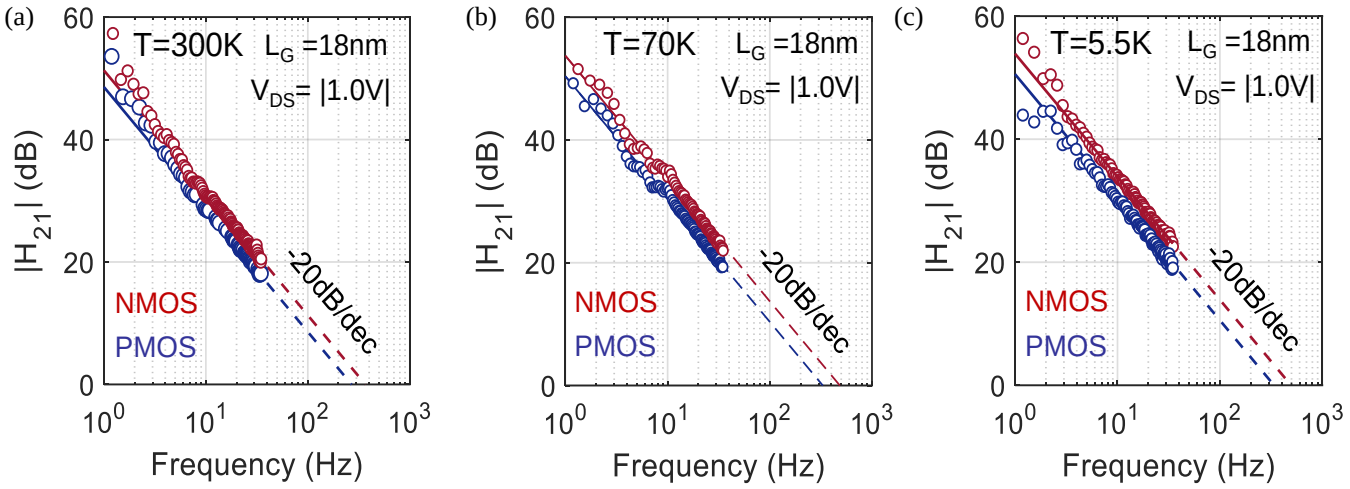

Fig. 4. Extraction of f_T from -20dB/dec extrapolation of access/pad parasitic de-embedded Short-circuit current gain ($|H_{21}|$) to unity, under peak-g_m gate bias and $|V_{DS}|$=1V for 18nm L_G NMOS (red) and PMOS (blue) at (a) 300K (b) 70K and (c) 5.5K

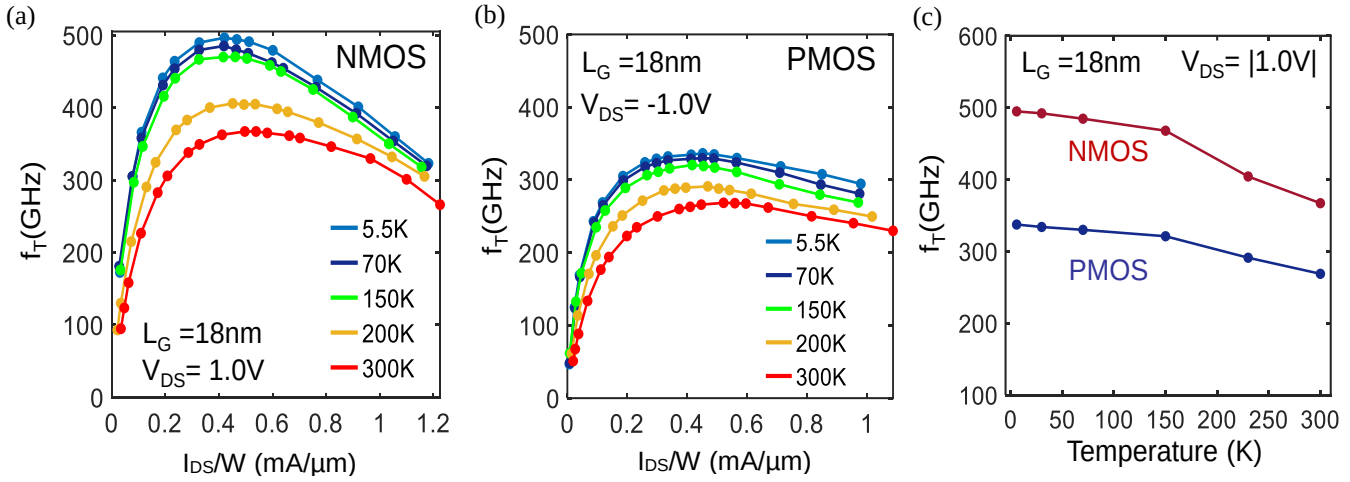

Fig. 5. Drain-current (I_{DS}/W) dependence of extrapolated f_T over the temperature range 300K to 5.5K for 18nm L_G (a) NMOS and (b) PMOS, under $|V_{DS}|$=1V. (c) Extrapolated Peak-f_T as a function of temperature show boost of 35% (to 495Ghz) and 25% (to 337GHz) at 5.5K for NMOS and PMOS respectively

Pad and Access parasitic de-embedded S-parameters were then used to extract the RF FoMs of the transistor, such as f_T and f_{MAX}. Subsequently, "cold" FET measurement at V_{GS}=0V was employed for both gate length structures to further de-embed the effect of extrinsic FET resistances [15]. Extrinsic FET capacitances were also de-embedded using the "cold" FET measurements in accumulation condition (at V_{GS}=-0.2/+0.2V for nFET/pFET), as explained in [15]. Finally, access and extrinsic FET parasitic de-embedded S-parameters were used to extract the intrinsic FET parameters at each bias point from the measurements in saturation condition.

III. Results and Discussions

A. *Cryogenic DC Characterization of 22nm FDSOI*

The well-tempered transfer characteristics (I_D-V_{GS}) of 18nm gate length (L_g) nFET and pFET from 300K down to 5.5K, are shown in Fig. 2(a,b) for linear (V_{DS}=50mV) and saturation region (V_{DS}=1V), respectively. The output characteristics with excellent saturation behavior (Fig. 2(c)) shows drain current (I_{DS}) improvement of 37% for nFET and 60% for pFET under iso-gate overdrive ($|V_{GS}$-$V_{T,\ Lin}|$=1V) at 5.5K compared to 300K. The linear ($V_{TH,\ Lin}$) and saturation ($V_{TH,\ Sat}$) region threshold voltage increase at cryogenic temperature for both nFET and pFET (Fig. 3(a), (b)), due to the increase in the fermi-potential at lower temperature [16]. $V_{TH,\ Lin}$ shift in SiGe pFET (160mV) was found to be more compared Si nFET (122.5mV) at 5.5K. However, the FD-SOI technology harnesses the back-gate biasing capability even at cryogenic temperature, which can be exploited to re-target the V_{TH} at low temperature. Fig. 3(c) shows the V_T tuning capability of the n-FDSOI MOSFET

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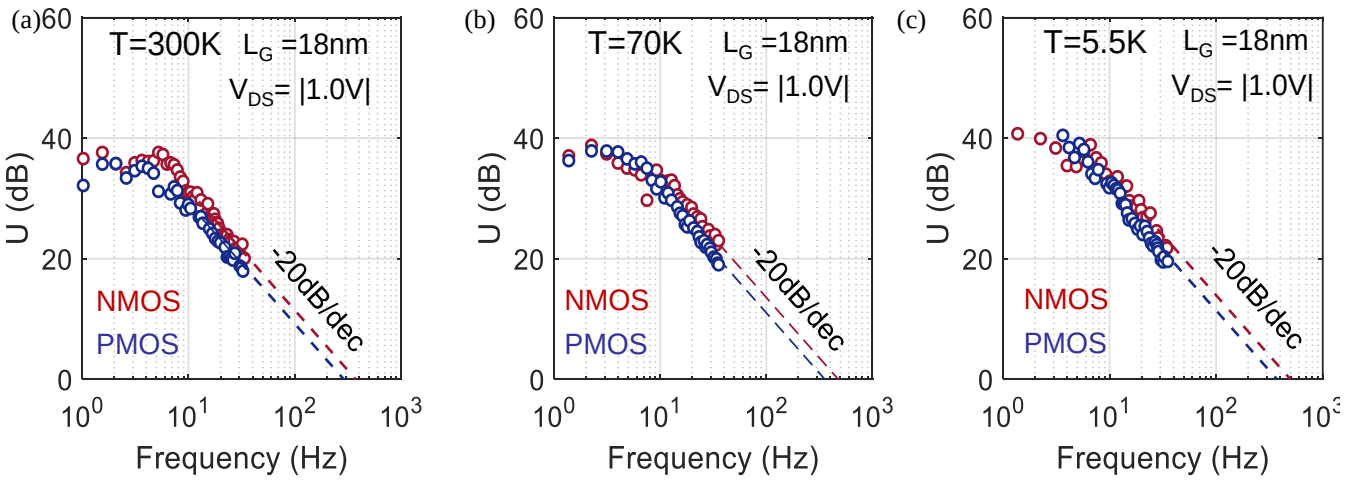

Fig. 6. Extraction of f_{MAX} from -20dB/dec extrapolation of access/pad parasitic de-embedded Unilateral power gain (|U|) to unity, under peak-g_m gate bias and $|V_{DS}|$=1V for 18nm L_G NMOS (red) and PMOS (blue) at (a) 300K (b) 70K and (c) 5.5K

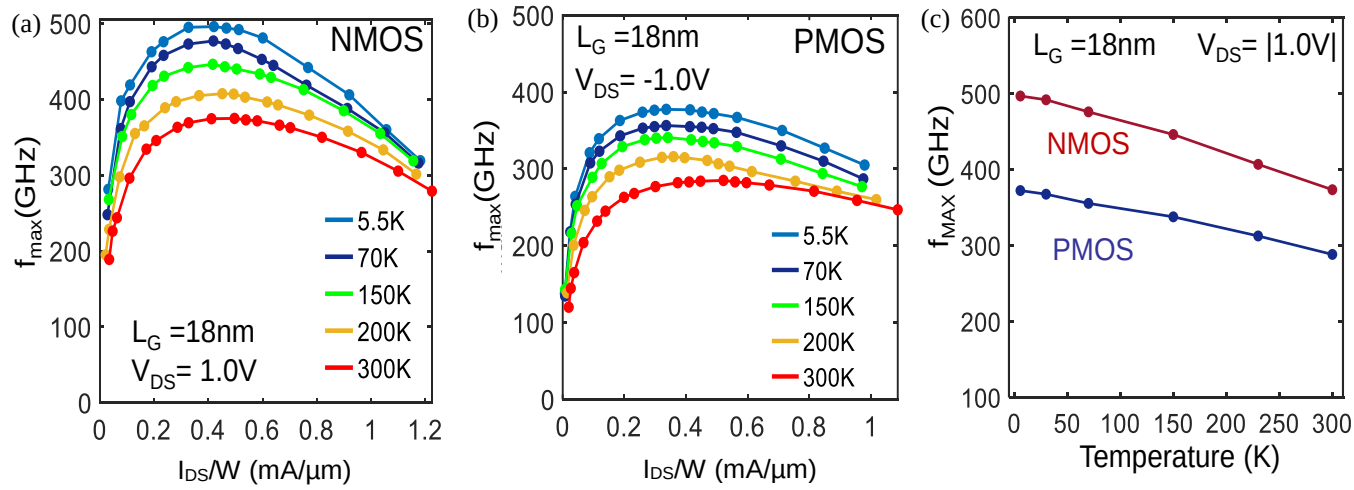

Fig. 7. Drain-current (I_{DS}) bias dependence of extracted f_{MAX} over the temperature range 300K to 5.5K for 18nm L_G (a) NMOS and (b) PMOS, under $|V_{DS}|$=1V. (c) Peak f_{MAX} as a function of temperature show f_{MAX} boost of 30% to 497 and 372 GHz at 5.5K for NMOS and PMOS respectively

at different temperatures. Back-bias voltage (V_B) of +2V is required to re-target the V_{TH} at 5.5K to that at 300K for 18nm NMOS FDSOI FETs. Interestingly, the back-biasing efficiency ($\gamma=\Delta V_T/\Delta V_B$) of n-FDSOI FETs was found to be constant across temperature (γ= -80mV/V). This indicates the highly doped p-well substrate does not undergo dopant freeze-out even at 5.5K. Subthreshold slope (SS), on the other hand, improves for both the NMOS and PMOS down to cryogenic temperature (Fig. 3(d)). However, SS do not scale linearly with temperature below 70K and saturate around 20mV/dec. This can be attributed to the location of Fermi-level close to high interface trap density (D_{it}) region, as well as sharp change in Fermi occupation function at cryogenic temperature, both leading to higher interface trap response capacitance (C_{it}) [17]. This results in sharp rise in the n-factor ($n=SS_{Experimental}/SS_{Ideal}$) below 70K with an inverse temperature dependence (T^{-1}), as shown in the inset of Fig. 3(d). The transconductance in saturation region ($g_{m,\,sat}$) is plotted as a function of the gate length (L_G), in Fig. 3(e) and 3(f) for nFET and pFET, respectively. $g_{m,\,sat}$ scales as $L_G^{-0.3}$ for both deeply-scaled (L_G< 50nm) nFET and pFET across all temperature. Improvement in $g_{m,sat}$ was found to be 33%/25% for nFET/pFET from 300K to 5.5K, across all channel length, due to reduced phonon scattering and improved source/drain contact resistance [12]. However, boost in $g_{m,\,sat}$ is saturated below 150K as carrier transport is dominated by temperature invariant surface roughness scattering. Also it should be noted that, $g_{m,\,Sat}$ in nFET FDSOI was found to saturate below 28nm gate length, whereas it continues to improve with L_G scaling in pFET FDSOI. This can be possibly due to the fact that $g_{m,\,Sat}$ at scaled gate length nFET is still dominated by the n+ Si source/drain contact resistance. However, this is not the case for Si-Ge channel PMOS since the source/drain contact resistance of p+ SiGe is lower compared to NMOS.

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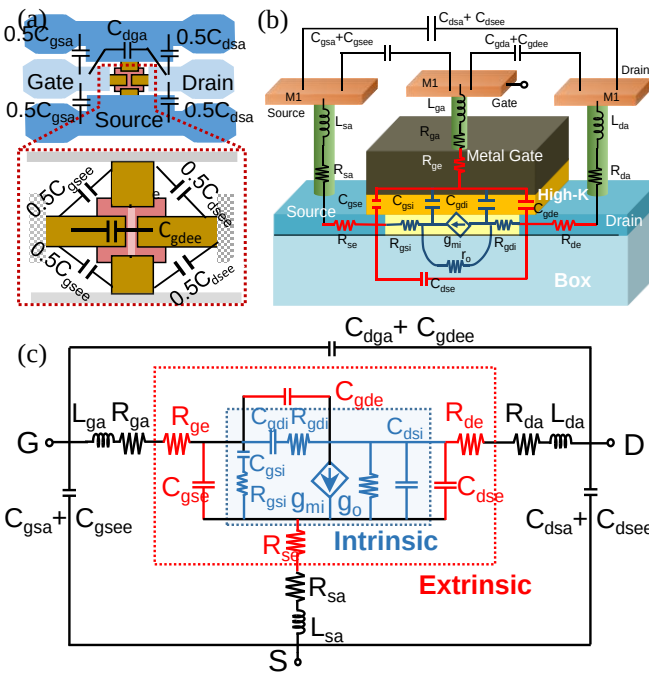

Fig.8: (a) Different access and pad parasitic in RF test structure; (b) Schematic view and (c) small-signal equivalent circuit model of 22nm FDSOI FET with illustration of access/interconnect parasitic, extrinsic and intrinsic FET elements

B. Cryogenic RF Characterization of 22nm FDSOI

Cryogenic RF characterization of 22nm FDSOI technology involves extraction of two main RF figures-of-merits (FoMs) as a function of drain current bias and operating temperature, namely transistor cut-off frequency (f_T) and maximum oscillation frequency (f_{max}). In order to extract f_T and f_{MAX}, access parasitic de-embedded S-parameters were used to calculate short-circuit current gain (H_{21}) and Mason's unilateral power gain (U), as mentioned in [10]. f_T was calculated through -20dB/dec extrapolation of H_{21} to unity gain ($|H_{21}|$=0dB), over a frequency range of 1GHz-20GHz. Fig. 4 shows the measured $|H_{21}|$ (symbols), under peak-g_m gate bias and $|V_{DS}|$=1V, along with -20dB extrapolation (line) for NMOS (red) and PMOS (blue) at (a) 300K, (b) 70K and (c) 5.5K. Similar method was followed to extrapolate f_T as a function of drain-current bias. Fig. 5(a, b) plot the drain-current dependence of extrapolated f_T for different temperature ranging from 300K to 5.5K for NMOS and PMOS respectively. Extrapolated Peak-f_T as a function of temperature shows, improvement of 35% from 367GHz at 300K to 494 GHz at 5.5K for NMOS and 25% from 268GHz at 300K to 337GHz at 5.5K for PMOS, as shown in Fig. 5(c).

Similarly, -20dB extrapolation of |U| to unity power gain ($|U|$=0dB) allows extraction of f_{MAX}. Fig. 6 plots measured |U| (symbols), under peak-g_m gate bias and $|V_{DS}|$=1V, along with -20dB extrapolation (line) for NMOS (red) and PMOS (blue) at (a) 300K, (b) 70K and (c) 5.5K. Drain current bias dependence

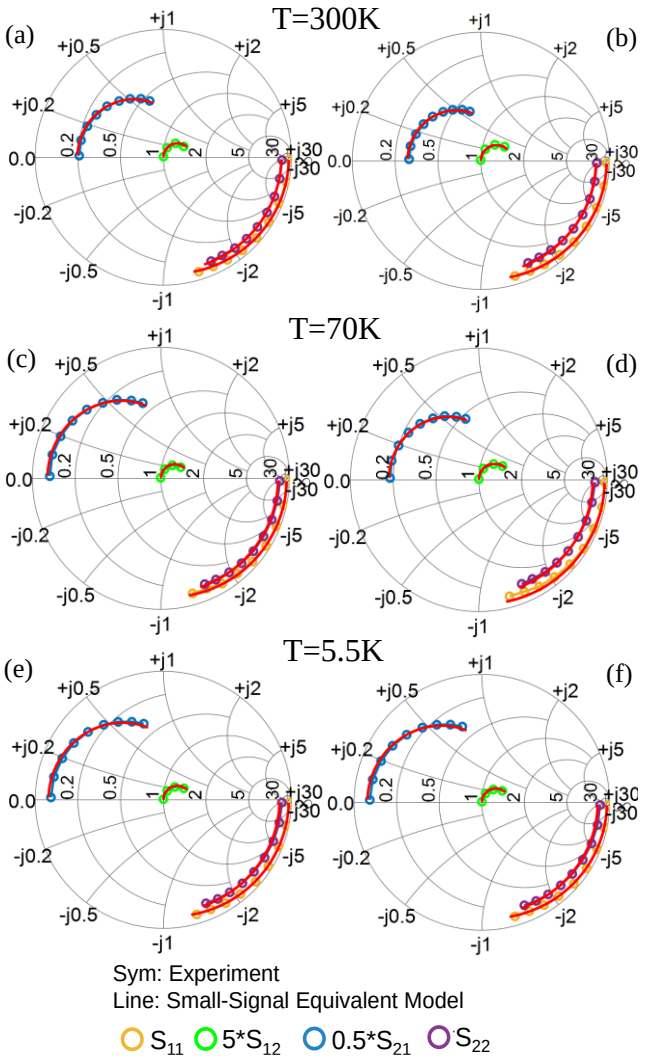

Fig. 9: Modeled (solid line) S-parameters using small-signal equivalent circuit model show perfect agreement with measured S-parameters (symbol) from 0.5-35 GHz for 18nm gate length n-FDSOI at (a) 300K, (c) 70K, (e) 5.5K and p-FDSOI at (b) 300K, (d) 70K, (f) 5.5K for V_{DS} = 1.0 V and V_{GS} at maximum gm

of extrapolated f_{MAX} across temperature is also extracted for NMOS (Fig. 7(a)) and PMOS (Fig. 7(b)). Extrapolated Peak-f_{MAX} was found to improve by 30% for both NMOS (from 373GHZ at 300K to 497GHz at 5.5K) and PMOS (from 288GHZ at 300K to 372GHz at 5.5K), as shown in Fig. 7(c). Accuracy of the de-embedding method used in this work is validated by the excellent agreement of extrapolated f_T and f_{MAX} at 300K with reported values for 22nm FDSOI FETs (nFET/pFET f_T 350/244GHz, nFET/pFET f_{MAX} 370/277GHz) [18]. It should be noted that drain current densities (I_{DS}/W) corresponding to both extrapolated peak-f_T and peak-f_{MAX} are invariant of temperature. This enables optimization space for cryogenic RF circuit designing, with operating either at 5x lower drain current bias for same f_T, f_{MAX}, at 5.5K compared to

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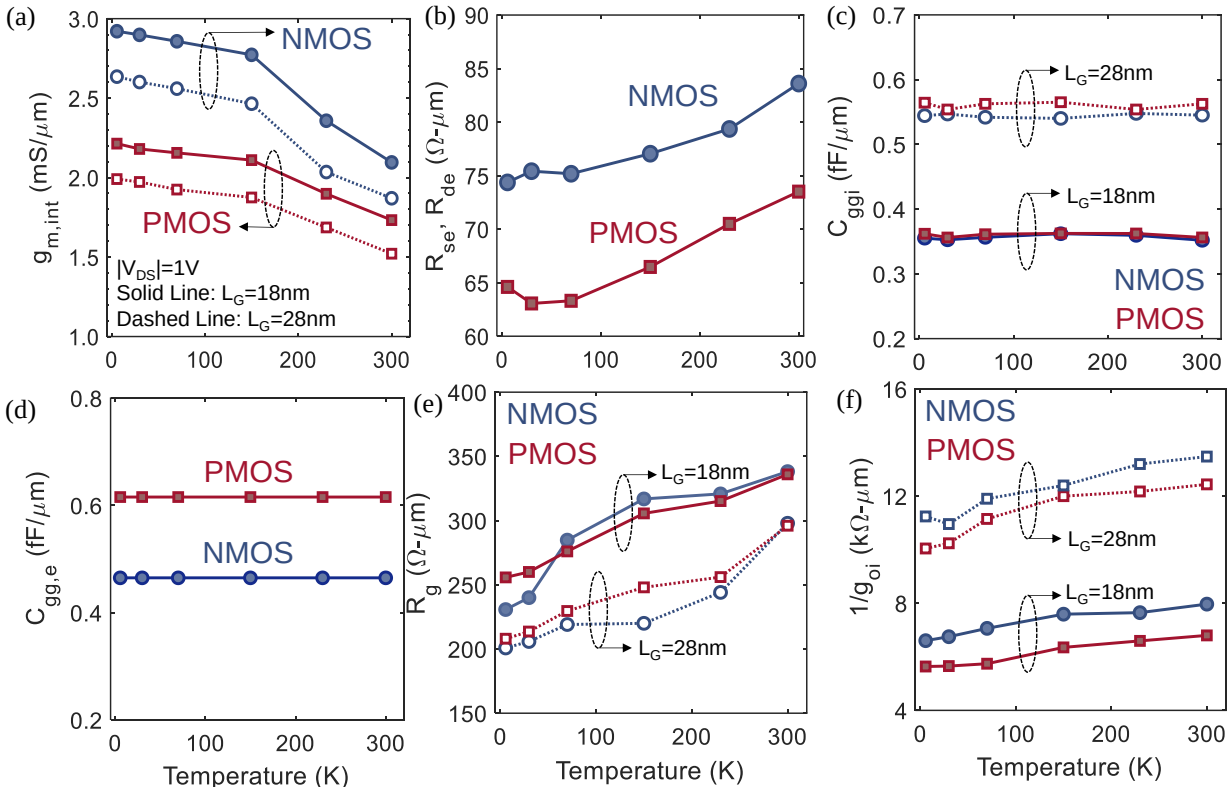

Fig. 10. (a) Intrinsic g_m ($g_{m,\ int}$) improves at low temp. in NMOS and PMOS due to reduced phonon scattering; (b) Source/drain series resistance ($R_{se,}$ R_{de}) improve by 15% at 5.5K; (c) Intrinsic ($C_{gg,i}$) and (d) extrinsic ($C_{gg,e}$) component of gate-capacitance ($C_{gg,T} = C_{gg,i}+C_{gg,e}$) remains invariant with temperature; (e) Reduced resistivity of gate metal contact (NiSi) and poly-Si cause gate resistance (R_{ge}) reduction at cryogenic temperature; (f) channel conductance (g_o) increase by 25% at low temperature

300K, or maintaining constant current bias (~500μA/ μm) across all temperature with higher f_T, f_{MAX} at low temperature.

Now, in order to understand the physical origin of the RF performance improvement and identify ultimate performance limit of cryo-RF FDSOI FET, small-signal equivalent circuit modeling and delay-time analysis are further performed, as discussed in the following sections.

C. Small-Signal Circuit Model for Cryogenic FDSOI

A small-signal equivalent circuit model was used to capture the Cryogenic RF performance of 18nm and 28nm L_G FETs for a bias condition of $|V_{DS}|$=1V and a $|V_{GS}|$ corresponding to the peak-g_m. Fig. 8(a) summarizes the access parasitic capacitances embedded within the RF test structure, along with interconnect-line parasitic, extrinsic and intrinsic FET parameters, shown in Fig. 8(b). The reference plane for the available RF test structure is M1 metal layer. The small-signal equivalent circuit model includes interconnect-line and access parasitic, along with extrinsic and intrinsic FET elements for accurately extracting RF figures-of-merit of 22nm Cryogenic FDSOI technology, as shown in (Fig. 8(c)). Extrinsic FET circuit elements include external resistances (R_{de}, R_{se}, R_{ge}) and capacitances (C_{gse}, C_{gde}, C_{dse}) associated with individual FET terminals, whereas intrinsic FET parameter set consists of intrinsic transconductance ($g_{m,int}$), intrinsic terminal capacitances (C_{gsi}, C_{gdi}, C_{sdi}) and output conductance (g_o). Measured and modeled S-parameters for 18nm L_G NMOS and PMOS show excellent agreement across the entire temperature range, as highlighted in Figs. 9 (a)-(f). The access capacitance and inductance elements were found to be temperature invariant, whereas interconnect-line resistance reduced at low temperature. However, due to infinitesimally low value (<3 ohm), these parameters were not found to have significant effect on the measured S-parameters across temperature.

Small-signal equivalent model parameters for 18nm L_G n & p FDSOI at 300K, 70K and 5.5K are listed in TABLE I. Fig. 10 summarizes the temperature and gate length dependence of small-signal equivalent model parameters. The intrinsic g_m improves by 39%/28% for NMOS/PMOS due to reduced phonon scattering at low temperature [19], as shown in Fig. 10(a). However, surface roughness (SR) scattering slows the rate of improvement in $g_{m,\ int}$ below 150 K, which is also

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TABLE I: Extracted Extrinsic and Intrinsic parameters for RF small-signal model

		NMOS (L_G=18nm)			PMOS (L_G=18nm)		
Temp.		300K	70K	5.5K	300K	70K	5.5K
Extrinsic Parameters	R_{se}/R_{de} (Ω-μm)	83.59	75.17	74.36	73.51	63.31	64.61
	R_{ge} (Ω-μm)	338	285	231	336	276	256
	C_{gse} (fF/μm)	0.233	0.233	0.233	0.312	0.312	0.312
	C_{gde} (fF/μm)	0.164	0.164	0.164	0.27	0.27	0.27
	C_{dse} (fF/μm)	$3.2x10^{-3}$	$3.2x10^{-3}$	$3.2x10^{-3}$	$6.2x10^{-3}$	$6.2x10^{-3}$	$6.2x10^{-3}$
Intrinsic Parameters	g_{mi} (mS/μm)	2.1	2.86	2.92	1.73	2.16	2.21
	$1/g_{oi}$ (kΩ-μm)	7.96	7.05	6.60	6.80	5.73	5.63
	R_{gsi} (Ω-μm)	0.12	0.090	0.075	0.12	0.090	0.075
	R_{gdi} (Ω-μm)	0.80	0.69	0.38	0.80	0.69	0.38
	C_{gsi} (fF/μm)	0.352	0.355	0.356	0.356	0.361	0.361
	C_{gdi} (fF/μm)	$1.2x10^{-4}$	$1.2x10^{-4}$	$1.2x10^{-4}$	$6.2x10^{-4}$	$6.2x10^{-4}$	$6.2x10^{-4}$
	C_{dsi} (fF/μm)	$1.2x10^{-4}$	$1.2x10^{-4}$	$1.2x10^{-4}$	$1.2x10^{-4}$	$1.2x10^{-4}$	$1.2x10^{-4}$

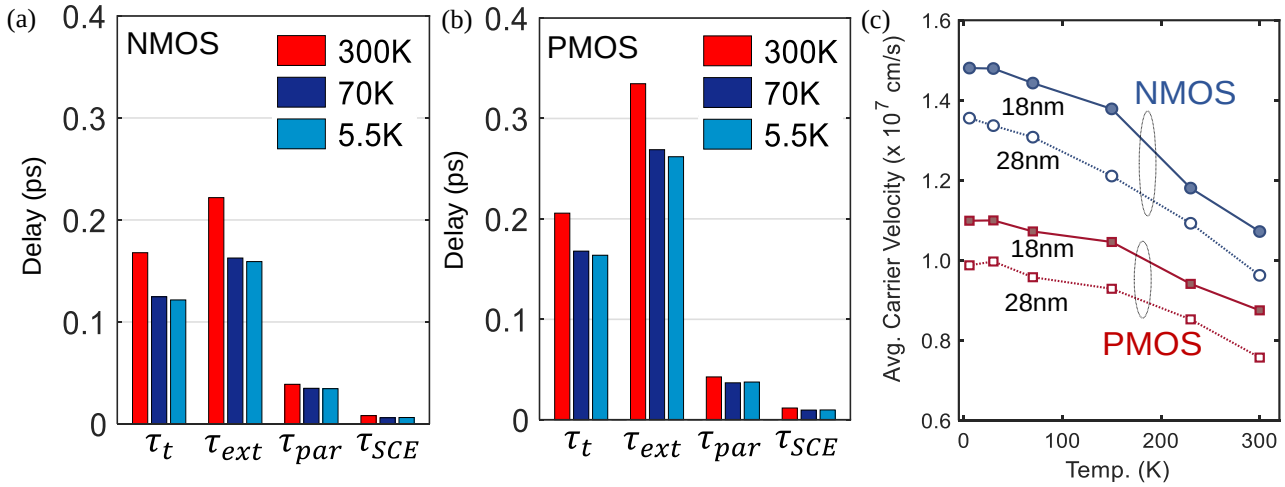

Fig. 11. Delay-time analysis shows 38%/25% improvement in intrinsic transit time (τ_t) and 40%/27% improvement in external parasitic delay (τ_{ext}) at 5.5K compared to 300K for 18nm L_G (a) NMOS and (b) PMOS respectively, (c) Improved transit time can be attributed to enhanced average electron and hole velocity at cryogenic temperature in NMOS and PMOS respectively

consistent with the cryogenic measurement result. Source-drain series resistance (R_{se}, R_{de}) are found to be invariant of gate length and improves by 11%/12% for NMOS/PMOS at low temperature due to reduced sheet resistivity of source/drain extension [20], but saturates below 100K (Fig. 10b). Simultaneous improvement in $g_{m,\,int}$ and R_{se}, R_{de} contributes to the observed boost in f_T. $C_{gg,i}$ scales with gate length whereas $C_{gg,e}$ has no gate length dependence (Fig. 10(c,d)). Both the intrinsic and extrinsic gate capacitances ($C_{gg,i}$ and $C_{gg,e}$ respectively) remain almost invariant with temperature for NMOS and PMOS, whereas the gate-resistance (R_{ge}) decreases monotonically by 32%/24% for NMOS/PMOS (Fig. 10(e)) due to reduced resistivity of gate metal contact (NiSi) and poly-Si at cryogenic temperature [21]. The combined effect of improvement in f_T and R_{ge} explains the improvement in f_{MAX} at low temperature. Output conductance (g_o) however increases at low temperature (Fig. 10(f)), due to slightly degraded short channel effect (SCE) likely from partial channel dopant de-activation in the channel.

However, small-signal equivalent circuit model parameters for Cryogenic-RF FDSOI were extracted with reference to M1 (metal 1) plane. Hence, it should be noted that effective values of the model parameters and also extracted f_T/f_{MAX} may vary depending on the connection of the extrinsic transistor to different metal layers present in an actual circuit. Cryogenic characterization and circuit model implementation of different

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TABLE II: Performance Benchmarking of Advanced Node Cryogenic-CMOS Technology

	28nm Bulk-Si [IEDM'19] [20]	**14nm FinFET [VLSI'20] [25]**	**28nm FDSOI [ESSDERC'17] [26]**	**28nm FDSOI [JEDS'20] [10]**	**22nm FDSOI [RFIC'19] [11]**	**22nm FDSOI [This work]**
L_G (nm)	30	15-23	28	25	20	18
V_{DD} (V)	0.8	0.75	0.9	1.0	0.8	1.0
n/p SS at 77K (mV/dec)	30/36	25/26	25/25	-	-	26/28
n/p $g_{m,\ Lin}$ @77K	+37%/+35 %	+55%/+49%	+66%/+67%	-	-	+60%/+71%
n/p $g_{m,\ Sat}$@77K	+19%/20%	+24%/+16%	+27%/+35%	33%/ -	+30%/+27%	+38%/+27%
n/p f_T (GHz)	-	-	-	400/- (at 4.2K)	380/240 (at 3.3K)	495/337 (at 5.5K)
n/p f_{Max} (GHz)	-	-	-	225/- (at 4.2K)	225/155 (at 3.3K)	497/372 (at 5.5K)

interconnect layer is hence required to allow accurate design of Cryogenic-RF CMOS. Also, intrinsic transconductance ($g_{m,i}$) in this work has been considered as a real number. However a phase factor associated with $g_{m,i}$ can also be included for capturing the non-quasi-static response of the small-signal equivalent circuit model [22], in order to allow operation at higher frequencies (>100GHz).

D. Delay-Time Analysis of Cryogenic-RF FDSOI

Delay-time analysis is performed to identify the contribution of different delay subcomponents on f_T improvement at 22nm FDSOI FETs at cryogenic temperature [23]. The analytical expression of f_T can be obtained from the small-signal equivalent circuit model as,

$$2\pi f_T = \frac{g_{m,i}}{C_{gg,T} + g_{m,i}R_{sde}\left[C_{gdi} + C_{gde} + \frac{g_o}{g_{m,i}}(C_{gg,T})\right]} \quad \ldots(2)$$

The total delay ($\tau_{Delay} = 1/2\pi f_T$) can hence be partitioned into four components, such as intrinsic transit time (τ_t), extrinsic charging delay (τ_{ext}), parasitic delay (τ_{par}) and delay due to short-channel effect (τ_{SCE}) :

$$\tau_{Delay} = \tau_t + \tau_{ext} + \tau_{par} + +\tau_{SCE} \quad \ldots(3)$$

where, $\tau_t = \frac{C_{gg,i}}{g_{m,i}}$, $\tau_{ext} = \frac{C_{gg,e}}{g_{m,i}}$, $\tau_{par} = R_{sd,e}.C_{gd,e}$ and $\tau_{SCE} = \frac{R_{sd,e}.(C_{gg,Ts}).g_o}{g_{m,i}}$.

Individual delay components for 300K, 70K and 5.5K, as plotted in Fig. 11 (a, b) for NMOS and PMOS respectively, reveal that all the delay subcomponents improve at 5.5K compared to 300K. Transit time (τ_t) can be calculated as the ratio of channel length (L_{Ch}) and average velocity of carriers (v_{Avg}) in the channel. Hence, the observed improvement in transit time can be attributed to enhanced average carrier velocity at cryogenic temperature for both NMOS and PMOS [24]. Fig. 11(c) summarizes the enhancement in v_{Avg} due to faster electron and hole transport in n and p-MOSFETs (L_G 18nm and 28nm) respectively. Improvement in $g_{m,\ int}$ enables reduction in τ_{ext} as $C_{gg,\ e}$ remains invariant with temperature. τ_{par} also scales with temperature due to reduced R_{se}, R_{de}. Moreover, τ_{SCE} improves down to 70K due to improved $g_{m,\ int}$ but slightly degrades at lower temperature as g_o also increases. Fig. 11(c) summarizes the percentage contribution of individual delay components on f_T improvement at 5.5K compared to 300K, for 22nm Cryogenic RF FDSOI. Reduced τ_{ext} at low temperature was found to have the most dominant effect on f_T improvement (54.5% for NMOS and 59.8% for PMOS), followed by improvement of τ_t (40.2% for NMOS and 34.4% for PMOS). Improvement in τ_{par} and τ_{SCE} were also found to have non-negligible effect on overall f_T boost. Hence reducing the extrinsic device parasitic capacitance (low-k spacer), reducing source/drain series resistance and improving SCE through thinner body, scaled EOT are potential pathways to further improve the RF performance of 22nm FDSOI technology at cryogenic temperature.

IV. CONCLUSION

In this work, we demonstrate record RF FoMs such as, f_T of 495/337 GHz and f_{MAX} of 497/372 GHz for NMOS/PMOS at 5.5K, on 22nm FDSOI platform. This improvement is attributed to 39%/28% boost in intrinsic g_m as well as 11%/12% lower source-drain external series resistance (R_{se}, R_{de}) and 32%/24% lower gate resistance (R_{ge}) for NMOS/PMOS at cryogenic temperature. Output conductance increased by 17% for both NMOS and PMOS at cryogenic temperature, with no significant effect on f_T. Furthermore, Back-biasing capability of 22nm FDSOI technology can be utilized for V_{TH} tunability at cryogenic temperature. Small-signal equivalent circuit model was used to extract the temperature variation of intrinsic and extrinsic transistor parameters for 22nm FDSOI technology down to deep-cryogenic temperature (5.5K). This paves a pathway for design-space exploration of high gain-bandwidth mixed-signal circuits for cryogenic RF applications. Performance benchmarking of Cryogenic CMOS technologies, as listed in TABLE II, reveal 22nm cryogenic-RF FDSOI FETs

showcased in this work provide superior f_T, f_{MAX} for both NMOS and PMOS, and hence is an excellent option for achieving superior analog performance with high transistor density at cryogenic temperature.

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