Power Performance Analysis of Digital Standard Cells for 28nm Bulk CMOS at Cryogenic Temperature using BSIM models

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***Abstract*— Cryogenic CMOS is a crucial component in building scalable quantum computers, predominantly for interface and control circuitry. Further, high performance computing can also benefit from cryogenic boosters. This necessitates an in-depth understanding of the power and performance trade-offs in cryogenic operation of digital logic. In this paper, we analyze digital standard cells in 28nm High-K Metal Gate (HKMG) CMOS foundry Process Design Kit (PDK). We have developed BSIM4 models of cryogenic CMOS and calibrated with experimental measurements. Since, low temperature operation leads to an exponential decrease in the leakage current of the transistors, we further tune the threshold voltage of the devices to achieve iso-leakage. In this paper, we present inverter static and dynamic characteristics and multiple Ring Oscillator(RO) structures. The simulation study shows that we can achieve 28%(FO4-RO) – 59%(NAND3-RO) higher performance under iso-VDD scenario and up to 90% improvement in the Energy Delay Product (EDP) under iso-overdrive scenario at 6K compared to room temperature.**

***Index Terms*— BSIM4, Cryogenic CMOS, Ring Oscillators, Standard Cells, Static Characteristics, Threshold Voltage, Transient Analysis.**

I. Introduction

Cryogenic CMOS (Cryo-CMOS) plays a key role in several applications like space electronics, astronomical detectors, metrology, high-performance computing and interface circuits to quantum computers [1]- [7]. The qubits operate in the deep cryogenic regimes of the order of few millikelvin. This operating temperature is dictated by both the implementation requirements of qubits (for ion traps, superconducting, spin etc.,) as well as reliability in terms of fidelity. A feasible solution for building a scalable quantum computer with reasonable number of interconnects is to place the control electronics and memory circuits closer to the qubits at around 4K rather than at room temperature [8] which will require digital, analog and RF circuits to operate at low temperatures. CMOS is one of the more reliable technologies that can provide an integrable solution with a higher number of qubits and operate at cryogenic temperature.

With remarkable improvement in the device behavior including ultra-low leakage current, higher ON current, near-ideal subthreshold swing, lower thermal noise and lower device and interconnect resistance [22], Cryo-CMOS has shown promising results for achieving higher performance and/or obtaining better power efficiency [2], [15]. Design requires well calibrated transistor models for low temperature operation, that can be used for circuit level simulations. There have been quite a few attempts to model the behavior of CMOS at low temperatures including but not limited to physics based semi-empirical models, simplified-EKV models, virtual source (VS) models etc., [9-13], [23-26]. There is a need for a physics based, accurate, scalable, robust MOSFET BSIM compatible model for circuit simulation and technology assessment. Some of the recent publications [16-20] demonstrate similar modelling but the devices are on matured technology nodes (E.g., 180nm).

In this paper, we introduce a BSIM4 MOSFET model compatible with cryogenic temperature for more recent 28nm bulk HKMG CMOS. The key transistor parameters are tuned to accurately model the device characteristics. The models are temperature dependent meaning the parameters are tuned for each temperature point in order to account for the varying device characteristics across the wide temperature range of 6K to 300K. The models are used to tune the transistor's threshold voltage to obtain iso-leakage at all the operating temperatures. The tuned BSIM4 models are then used to analyze the power and performance of digital standard cells with an emphasis on CMOS inverters and a family of ring oscillators.

The remainder of the paper is organized as follows. In Section II we examine some of the key transistor properties at low temperatures and briefly describe the BSIM4 modelling methodology. In Section III we analyze the performance and power metrics of digital standard cells and conclusions follow.

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II. Device Characteristics at Cryogenic Temperatures

The transistor device I_{ds}-V_{gs} and I_{ds}-V_{ds} for 28nm Gate First based High-K Metal Gate (HKMG) bulk Si NMOS and SiGe PMOS from Global Foundries [27] are measured on a Lakeshore CPX-VF cryogen-free cryogenic probe station from 300K to 4K. The devices have chemical oxide based gate oxide (Interlayer and Hafnium Oxide based High-k) and an equivalent oxide thickness (EOT) of 1.25nm. The device output characteristics for iso-overdrive voltage ($V_{ov} = |V_{gs}| - |V_{th}|$) of 0.5V is shown in Fig. 1 (a). We choose the iso-overdrive scenario for the following reason, since with decrease in temperature, the threshold voltage of the devices increases, in order to provide correct comparison of increase in current, it would be accurate to model the amount of charge accumulated after the device turns ON ($|V_{gs}| > |V_{th}|$) by a constant headroom (we choose a headroom or overdrive of 0.5V). The device transfer characteristics are shown for linear region (Fig. 1 (b)) defined by $|V_{ds}|$ = 50mV and saturation region (Fig. 1 (c)) defined by $|V_{ds}|$ = 1V. All the curves indicate increase in device ON current from 300K to 4K. As evidenced by the output characteristics, there is no kink effect for bulk 28nm CMOS. We also notice that the slope of the transfer characteristics

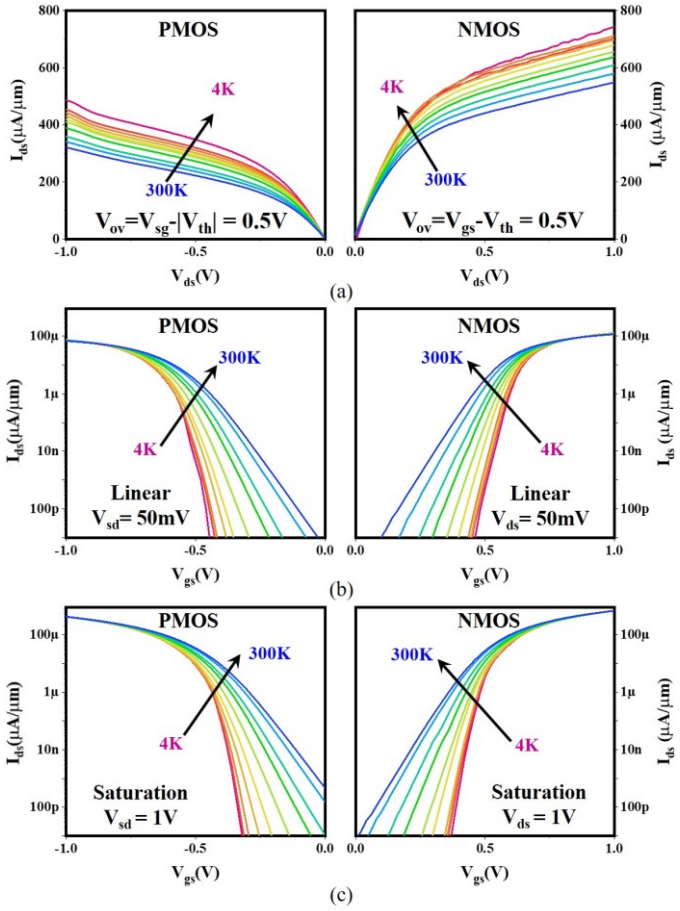

Fig. 1. Measured device characteristics across temperature showing (a) transistor output characteristics for iso-overdrive of 0.5V (b) transistor transfer characteristics in linear region defined by Vds = 50mV (NMOS) and Vsd = 50mV (PMOS) and (c) transistor transfer characteristics in saturation region defined by Vds = 1V (NMOS) and Vsd = 1V (PMOS).

becomes steeper with decrease in temperature and the device OFF current decreases exponentially (notice the log scale of Fig. 1 (b) and 1 (c)). This means the subthreshold swing of devices decreases linearly with temperature proving more ideal ON-OFF characteristics.

III. Device Modelling at Cryogenic Temperature

We use industry standard tool BSIMProPlus™ to calibrate BSIM4 model parameters to the measured data and analyze the fit parameters. The parameters are individually fit to five key temperature points (300K, 150K, 70K, 30K and 6K) so as to obtain lower error percentage. We tune minimal number of crucial parameters like V_{th0}, V_{SAT}, U0, K1, ETA0, DSUB, CIT and RDSW that control the device behavior. The Fig. 2. shows the flow of parameter tuning at a given temperature.

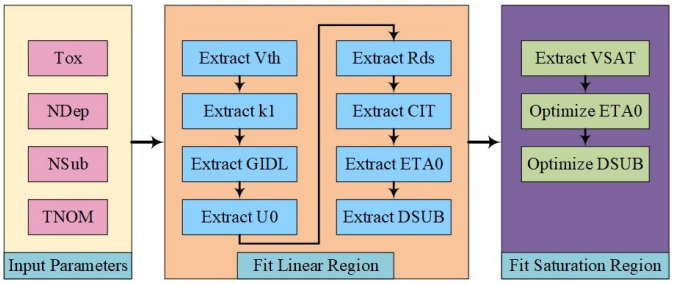

Fig. 2. Flow diagram for parameter tuning at each temperature point.

A. Threshold Voltage

The increase in the Silicon (Si) bandgap along with exponential scaling of Fermi-Dirac occupation function, decrease in intrinsic carrier concentration causing increased bulk Fermi potential and incomplete ionization all collectively cause the threshold voltage of the MOSFET to increase with decrease in temperature [21]. In BSIM4, the temperature dependence of threshold voltage is modelled by

$$V_{th}(T) = V_{th0}(TNOM) + \left(KT1 + \frac{KT1L}{L_{eff}} + KT2 \cdot V_{bseff}\right)\left(\frac{T}{TNOM} - 1\right) \quad (1)$$

KT1 is the dominant parameter to describe the temperature dependence of Vth, KT1L improves the fitting for various channel length sizes and KT2 models the temperature dependence of the body effect onV_{th0}. In our case, since we are fitting for a constant channel length and not studying the body effect, we retain the default values for KTL1 and KTL2 parameters. The final fit V_{th} is shown in Fig. 3 (a) and shows approximately 100mV shift from 300K to 6K.

B. Mobility and Velocity Saturation

The mobility of the charge carriers is degraded by the vertical electric fields in scaled nodes and at higher gate voltages which is further degraded by the phonon/surface roughness and Coulomb scattering. However, at lower temperatures, due to lower lattice vibrations, the phonon scattering largely reduces. On the other hand, the surface roughness under strong transverse electric field increases with decrease in temperature

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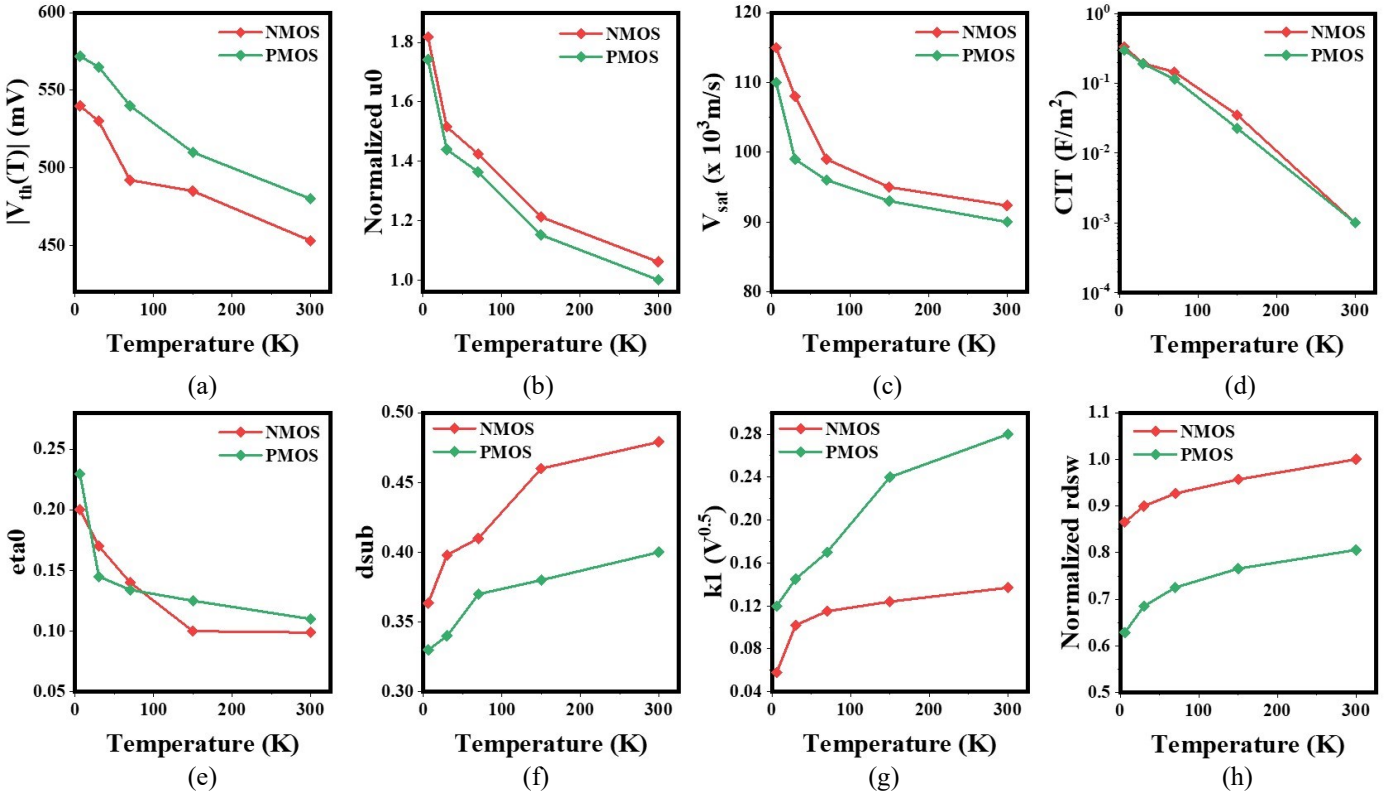

Fig. 3. Fitted BSIM4 parameters (a) Threshold Voltage (b) Normalized Low-Field Mobility (c) Saturation velocity (d) Interface Trap Charge (e) DIBL coefficient in subthreshold region (f) DIBL coefficient exponent in sub-threshold region (g) First-order body bias coefficient (h) Zero bias LDD resistance per unit width for RDSMOD=0 normalized to NMOS at 300K

as low temperature electrons have lesser kinetic energy making them more vulnerable to surface roughness scattering.

Coulomb scattering due to bulk charge increases with decrease in temperature since the interaction time between the fast moving channel carriers and ionized impurity centers becomes longer but is reduced at higher electric fields due to screening effect. Conversely, Coulomb scattering due to interface charges though higher gets masked by the reduced screening effect causing mobility due to Coulomb scattering from interface charge show inverse proportionality to temperature. These phenomena have been captured in the recent modifications to BSIM models [18] and the final effective mobility is given by

$$\mu_{eff} = \frac{\mu_0}{1 + U_A E_v^{E_U} + \frac{U_D}{\left[\frac{1}{2}\left(1 + \frac{U_{DS} q_s + U_{DD} q_d}{q_0}\right)\right]^{U_{CS}}}} \quad (2)$$

where q_s and q_d are normalized source- and drain- side inversion charge densities, q_0 is a temperature independent constant, E_v is the effective vertical electric field, μ_0, U_A, U_D, U_{CS}, U_{DS} and U_{DD} are temperature dependent mobility coefficients, all following linear temperature dependent power law as:

$$\mu_0(T) = \mu_0(T_{nom})(T_r)^{U_{01}+U_{02}T_r} \quad (2a)$$
$$U_A(T) = U_A(T_{nom})(T_r)^{U_{A1}+U_{A2}T_r} \quad (2b)$$
$$U_D(T) = U_D(T_{nom})(T_r)^{U_{D1}+U_{D2}T_r} \quad (2c)$$
$$U_{CS}(T) = U_{CS}(T_{nom})(T_r)^{U_{CS1}+U_{CS2}T_r} \quad (2d)$$

and E_U is the slope of μ_{eff} versus E_v.

$$E_U(T) = E_U(T_{nom}) + E_{U1}(T_r - 1) \quad (2e)$$

U_{01}, U_{02}, U_{A1}, U_{A2}, U_{D1}, U_{D2}, U_{CS1}, U_{CS2} and E_{U1} are all temperature independent parameters. In this work, we capture the effects by fitting U0 and the normalized U0 as a function of temperature is shown in Fig. 3(b).

A cubic polynomial temperature dependence model of velocity saturation parameter VSAT proposed in [18] to fit the nonlinear data has been used here. The variation of V_{SAT} with temperature is shown in Fig. 3 (c).

$$V_{SAT}(T) = V_{SAT}(TNOM) + A_T \Delta T + A_{T1} \Delta T^2 + A_{T2} \Delta T^3 \quad (3)$$

C. Subthreshold Slope and Drain Induced Barrier Lowering

The exponential dependence of I_D on temperature seen in (4) causes the subthreshold slope to become steeper with decreasing temperature. I_0 is the saturation current, k_B is the Boltzmann's Constant.

$$I_D \approx I_0 e^{\frac{q(V_{GS} - V_{th})}{n k_B T}} \quad (4)$$

$$SS = \left[\frac{\partial \log(I_D)}{\partial V_{GS}}\right]^{-1} = \ln(10) \frac{n k_B T}{q} \quad (5)$$

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where n is the non-ideality factor defined by

$$n = 1 + \frac{C_{dep}}{C_{ox}} + \frac{C_{it}}{C_{ox}} \quad (6)$$

C_{it} is the interface trap capacitance, C_{dep} is the depletion capacitance and C_{ox} is the oxide capacitance. However, the measured *SS* deviates from the Boltzmann limit below a critical temperature and then saturates to a value depending on the technology. The inclusion of interface trap capacitance $C_{it} \propto qN_{it}$ in the slope factor helps modeling the behavior up to ≈ 50K, but at deep cryogenic temperatures, leads to unreasonably high N_{it} values.

One other explanation is attributed to a more intrinsic mechanism of presence of localized trap energy states in the band tail in addition to the delocalized states that take part in conduction [28][29], revising the saturated value of SS when thermal energy becomes smaller than the band-tail extension (W_t) to a temperature independent $n \cdot \ln(10) \cdot (W_t/q)$ rather than $n \cdot \ln(10) \cdot (k_B T/q)$ below a critical temperature of ≈ 46K [11]. In this paper, SS trend has been captured and modelled with BSIM4 parameter CIT whose variation with temperature is shown in Fig. 3(d) and agrees with [30].

To fit the I_d-V_{gs}, we also tune the DIBL coefficient in the subthreshold regime ETA0, DIBL coefficient exponent in subthreshold regime DSUB and First order body bias coefficient k1 (Fig. 3(e), 3(f) and 3(g) respectively).

D. Drain Source Parasitic Resistance

The drain source parasitic resistance includes many contributing factors such as contact resistance, diffusion resistance between contact and gate, crowding resistance near gate etc. The BSIM4 parameter RDSW is used to characterize temperature dependence along with temperature coefficient PRT. The variation of fitted RDSW with temperature is shown in Fig. 3(h).

$$RDSW(T) = RDSW(TNOM) + PRT\left(\frac{T}{TNOM} - 1\right) \quad (7)$$

E. Model Validation

All these key parameters provide a closely fitted model with mean rms error of less than 4.24% at all temperature points. Fig. 3 shows the validated models for both NMOS and PMOS at the five temperature points with lines representing fitted BSIM4 models and points being experimental data. Fig. 4(a) shows the output characteristics for iso-overdrive voltage of 0.5V, Fig. 4(b) shows transfer characteristics for linear region and Fig. 4(c) shows transfer characteristics for saturation region. Fig. 5 shows the extracted gate capacitance values from the BSIM4 models which will be later used for simulating and predicting dynamic behavior of the digital standard cells in Section IV.

F. Threshold Voltage Tuning for Iso-Leakage Models

We use the above developed BSIM4 models to tune the threshold voltage across temperatures so that the devices have same subthreshold leakage current I_{OFF}. This is done by reducing the V_{th} at lower temperature so as to maximize the headroom or overdrive ($V_{ov} = V_{gs} - V_{th}$) and increase the ON current. It has been experimentally demonstrated from foundry process that metal gate work function tuning, metal-oxide cap induced interfacial dipole layers, and lower bandgap channel

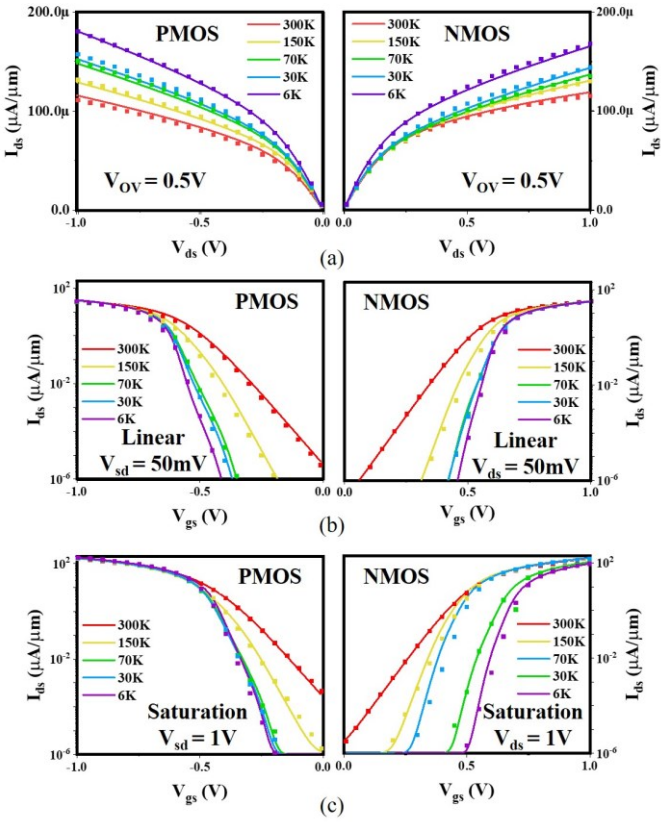

Fig. 4. Measured Device characteristics (points) and fitted BSIM4 model (solid lines) *after* V_{th} tuning for *iso-IOFF* of 1nA/μm (lower V_{th} for low temperature devices as per Fig. 6) as against Fig. 1 which illustrates raw measurements, showing (a) Output characteristics for constant overdrive of 0.5V, Transfer Characteristics for (b) Linear Region and (c) Saturation Region.

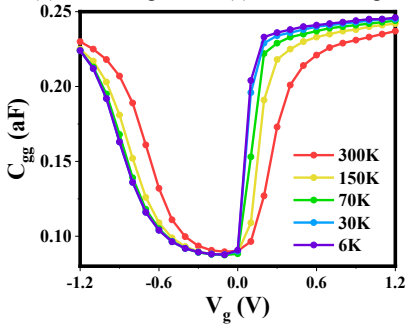

Fig. 5. Transistor Gate Capacitance Variation with temperature extracted from calibrated BSIM4 Models.

I_{OFF}	Type	300K	150K	70K	30K	6K
1nA/μm	NMOS	0.274	0.239	0.215	0.205	0.195
	PMOS	0.410	0.325	0.257	0.195	0.158
0.1nA/μm	NMOS	0.353	0.280	0.244	0.224	0.216
	PMOS	0.507	0.378	0.311	0.301	0.200
0.01nA/μm	NMOS	0.428	0.331	0.289	0.270	0.261
	PMOS	0.605	0.455	0.346	0.280	0.222

Fig. 6. Final engineered threshold voltage for different values of device-OFF currents (I_{OFF}). (Absolute values shown for PMOS devices)

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materials are amongst a few methods to achieve such V_{th} tuning [15]. For the rest of the paper, we use the Vth engineered BSIM4 models for our analysis and refer to it as "*Iso-I_{OFF} models*". The final tuned Vth values for NMOS and PMOS devices at the five temperatures for three values of device OFF currents I_{OFF} is shown in Fig. 6.

IV. Power And Performance Analysis of Digital Standard Cells

In this paper we discuss the behavior of INV, NAND2, NAND3, NOR2 and NOR3 gates simulated for industry standard 28nm technology node using the above developed Iso-I_{OFF} BSIM4 models. At cryogenic temperatures, many device properties change viz. (1) increase in threshold voltage, (2) increase in the saturation current, (3) exponential decrease in Sub-threshold leakage current or I_{OFF} etc., Hence, it becomes difficult to compare the performance and other figures of merits across temperature. Keeping one of the parameters constant will simplify the analyses. The rationale behind choosing Iso-IOFF is two-fold: (a) this will provide iso-leakage power analysis at low temperatures, (b) tuning devices for IOFF same as that at room temperature will reduce the threshold voltage at cryogenic temperature, providing more overdrive voltage and hence better performance as explained in the previous section. All the devices considered in the simulation are of 1x drive strength. The device sizes are shown in the Table I.

Table I. Standard Cells & Device sizes (1x drive strength)

Cell	NMOS	PMOS
INV	140nm	170nm
NAND2	140nm	170nm
NOR2	140nm	170nm
NAND3	140nm	170nm
NOR3	140nm	340nm

A. Inverter Static Characteristics

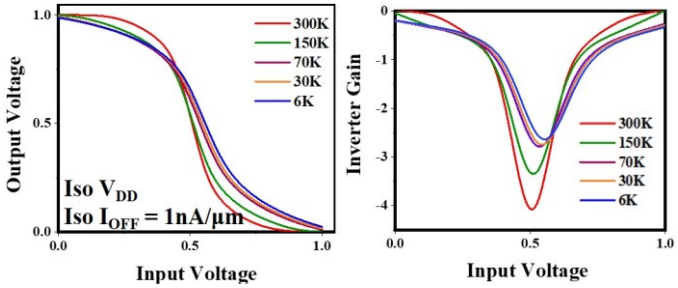
The inverter Voltage Transfer Characteristics (VTC) is shown in Fig. 7(a). The slope of the curve or the gain of the inverter decreases with decrease in temperature with peak gain reducing from -4.08 (300K) to -2.64 (6K) (35% decrease) due to the lower threshold voltage V_{th} of tuned devices and the input voltage corresponding to the peak gain increases by 4.2% of supply voltage V_{DD} (Fig. 7(b)). The plots in Fig. 8(a) show that the inverter trip voltage (V_M) increases with decrease in temperature. Ignoring the short channel effects, the trip voltage is related to the transconductance parameter $k = \mu CoxW/L$ as

$$V_M \propto \frac{r}{1+r} \tag{8}$$

$r = k_p/k_n$ is the ratio of PMOS and NMOS transconductances. The increase in current for PMOS is higher than that of NMOS (for Iso-IOFF devices) indicating change in mobility for PMOS is higher, thus explaining the upward shift of V_M.

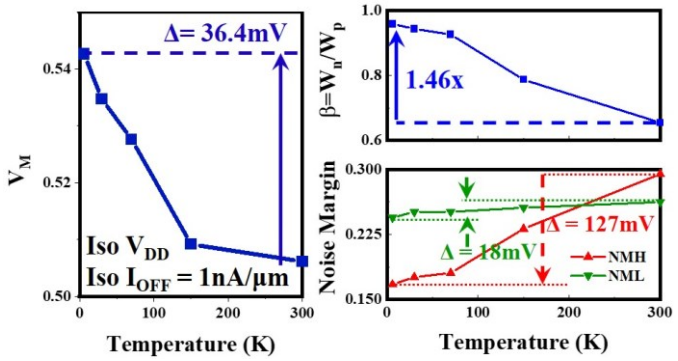
Also, due to the higher strength of PMOS at lower temperature, the β ratio needed to achieve $V_M = V_{DD}/2$ increases with decrease in temperature (Fig. 8(b) top) and the noise margins (NM) decreases (NM-High by 127mV and NM-Low by 18mV) with decrease in temperature (Fig. 8(b) bottom). In Fig. 9(a) the variation of input pin capacitance with input voltage for 1x inverter for different temperatures is shown. The total switched charge given by the area under curves Fig. 9(a) increases and at iso-V_{DD}, the input pin cap increases by approximately 12% going from 300K to 6K which is due to the increased charge inversion at the channel created by the larger overdrive voltage (V_{ov}) created in retargeted V_{th} devices (Fig. 9(b)).

$$Q_{SW} = \int_0^{V_{DD}} C(V)dv \tag{9}$$



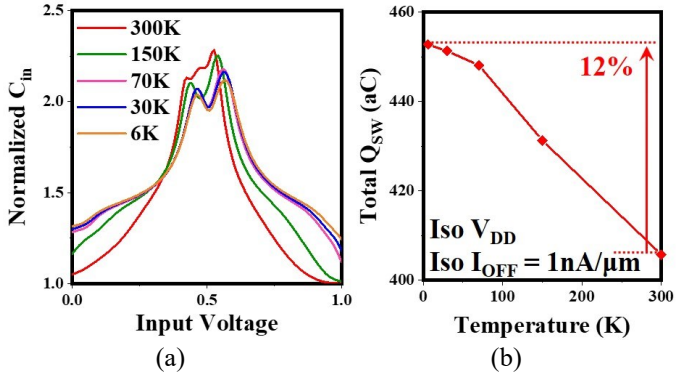
(a) (b)

Fig. 7. Simulated (a) Inverter Voltage Transfer Characteristics for iso I_{OFF} devices at Iso-V_{DD} across temperature and (b) resulting voltage gain for 1x Inverter. (Device Sizes: NMOS: 140nm/30nm PMOS: 170nm/30nm).



(a) (b)

Fig. 8. (a) Inverter trip voltage V_M for iso I_{OFF} devices at Iso-V_{DD} across temperature showing 36.4mV shift from 300K to 4K. (b) β needed to achieve $V_M = V_{DD}/2$ and noise margins for 1x inverter.



(a) (b)

Fig. 9. (a) Extracted input pin capacitance C_{in} for 1x inverter across temperature showing from simulation (b) Total switched charge Q_{SW} per input transition for 1x inverter at iso-I_{OFF} and iso-V_{DD} conditions showing 12% increase from 300K to 6K.

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B. Inverter Transient Characteristics

In the inverter transient characteristics, we see the variation of propagation delay t_{pd} (defined as time between 50% of input and output transitions) for different Fan-Out (FO) conditions (Fig. 10). We observe between ~24% (FO=9) -28\% (FO=1) improvements in the same. The switching speed increase is a direct effect of increased ON current at lower temperatures with additional current increase from V_{th} retargeting. The variation of delay with supply voltage across temperature for a 1x inverter is shown in Fig. 11. The transient variation of inverter short circuit current I_{SC} during the switching activity is plotted in Fig. 12(a). One of the key take-away from [2] was that the internal power of the system increases by 77% going from 300K to 100K. This can be clearly explained from the BSIM4 models where we notice that I_{SC} increases going from 300K to 6K due to higher I_{ON} with ~20% increase in the peak value for input slew of 20ps for a 1x inverter driving a nominal 1fF load.

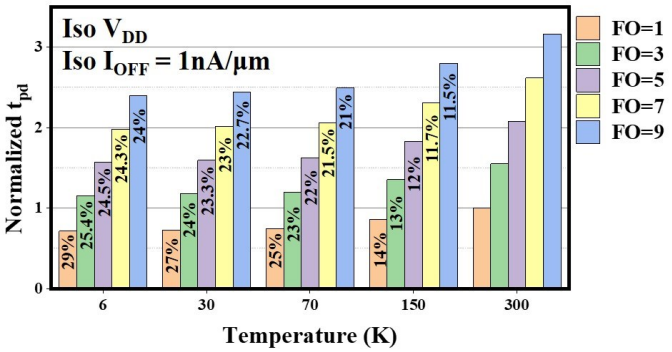

Fig. 10. Simulated propagation delay of 1X inverter for different fanout conditions at Iso-VDD and iso-IOFF conditions across temperature normalized to FO =1 at 300K. t_{pd} defined as time between 50% input and output transitions. The percentage reduction from room temperature is shown for lower temperatures.

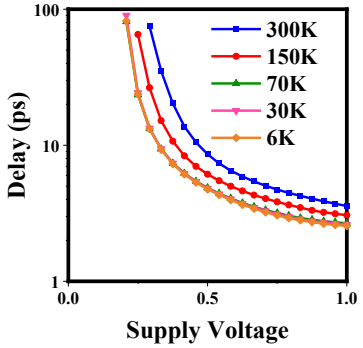

Fig. 11. Delay versus supply voltage for 1x inverter across temperature.

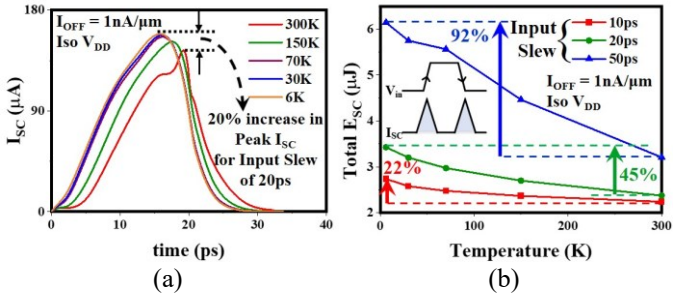

Fig. 12. (a) Transients of input short circuit current I_{SC} for 1x inverter with input slew of 20ps across temperature showing peak I_{SC} increase by 20% from 300K to 6K. (b) Total Short Circuit Energy E_{SC} per transition of input for 1x inverter across temperature at different input slew rates indicating lower increase in E_{SC} for sharper slew conditions at 6K.

The short circuit power which is a function of the input slew increases between 22% for 10ps slew, 44.5% for 20ps slew and 92% for 50ps slew (Fig. 12(b)).

C. Ring Oscillators

We design multiple ring oscillator structures based on NAND2, NOR2, NAND3, NOR3 and FO4 inverters to obtain the frequency of oscillation at the five key temperature points. We see improvements of 28% for FO4, 32% for NOR2, 37% for NOR3, 40% for NAND2 and 59% for NAND3 in the frequency of oscillation compared to their corresponding 300K values (Fig. 13) and the rise/fall times normalized to that of FO4 values at 300K is shown in Fig. 14.

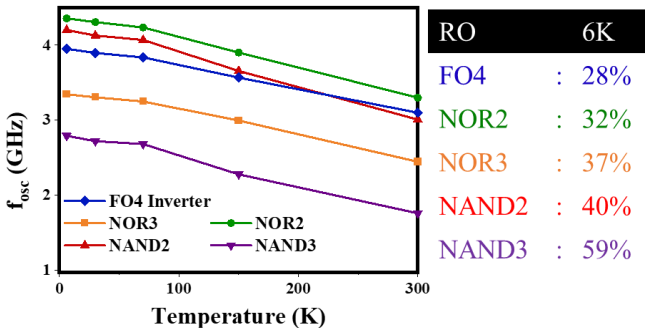

Fig. 13. Frequency of oscillation from simulation for different ring oscillator structures across temperature at Iso-V_{DD} and Iso-I_{OFF} conditions and percentage improvement at 6K compared to 300K.

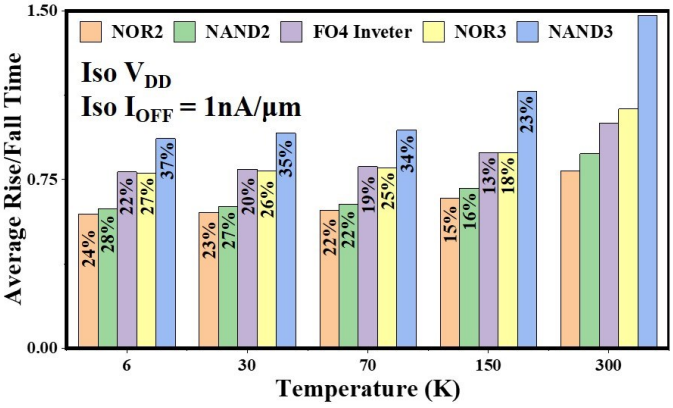

Fig. 14. Average rise/fall times extracted from ring oscillator frequency across temperature, normalized to 300K FO4 inverter, at iso-V_{DD} and Iso-I_{OFF} conditions.

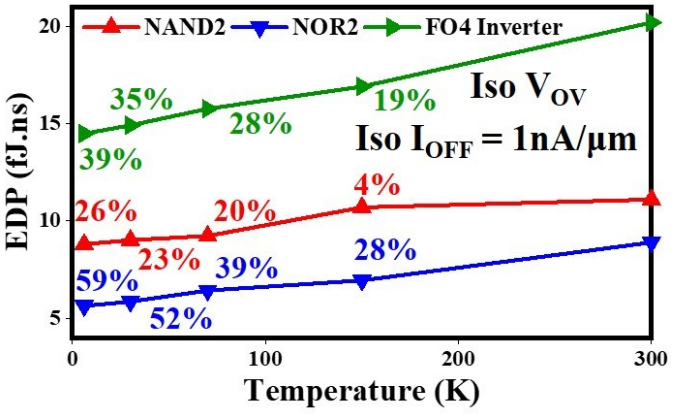

Fig. 15. Energy Delay Product (EDP) improvement for 3 RO structures across temperature at Iso I_{OFF} and Iso-Overdrive (V_{OV}) conditions.

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One of the key advantages of operating CMOS at cryogenic temperature is that we can overcome the VDD scaling limits to operate the devices at lower supply voltages, while still achieving better performance compared to room temperature, thus saving power. Fig. 15 shows the EDP improvements at Iso-Overdrive (Iso-Vov) scenario. Fig. 16 shows the supply voltage needed at lower temperatures to achieve oscillation frequency observed at 300K and the corresponding performance/watt. We see between 1.7X-1.9X improvement between 300K and 6K.

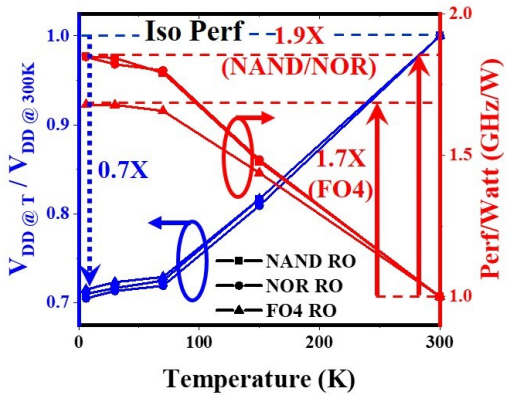

Fig. 16. Normalized Supply Voltage needed to achieve oscillation frequency of 300K RO and corresponding performance per watt improvements.

V. Conclusion

In this paper, we use BSIM4 models with Vth tuning for achieving iso-I_{OFF} to characterize primitive standard cells and show through exhaustive simulations that we can achieve up to 90% performance/watt improvement by operating CMOS at 6K. The analysis of the cost of cooling is beyond the scope of this paper and it will add significant overhead. The BSIM4 models provide a pathway for developing a full PDK at cryogenic temperatures which can be used to accurately predict and design cryogenic circuits and systems. the importance of the work or suggest applications and extensions.

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