A 94% Peak Efficiency 48-to-1-V GaN/Si Hybrid Converter With Three-Level Hybrid Dickson Topology and Gradient Descent Run-Time Optimizer

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***Abstract*— This work presents a direct 48–1-V DC–DC point-of-load (POL) converter for efficient high-voltage conversion. Conventional hybrid topologies face limitations of large number of off-chip components and limited operation ranges. By combining the three-level buck converter with the hybrid Dickson converter, the proposed topology shows ten times reduced switching voltages with only five off-chip flying capacitors—a near 50% reduction compared with prior works. The reduced voltage stress enables using low-voltage on-chip Si power devices, further reducing the number of off-chip switches. A gradient descent run-time optimizer along with a hybrid current-sensing analog-to-digital converter (ADC) is proposed to dynamically optimize converter's efficiency, improving the operation range. Thus, the proposed design overcomes the limitations of previous hybrid converters. The prototype was fabricated using a 0.18-μm Bipolar-CMOS-DMOS (BCD) process. The converter achieves an input voltage of 48 V and an output voltage of 0.7-to-1 V with a maximum load capacity of 12 A. The measured peak efficiency is 90.4% at 48–1-V conversion, and the maximum efficiency improvement is 16.7% with the proposed optimization circuits.**

***Index Terms*— 48–1 V, DC–DC converter, digital control, hybrid converter, hybrid Dickson, optimization, point-of-load (POL) converter.**

I. Introduction

With the proliferation of artificial intelligence (AI), cloud computing, and the Internet of Things (IoTs), the power demanded in data centers is growing rapidly. In response to this, the power delivery in data centers is moving from the conventional 48–12–1-V multistage conversion to the 48–1-V direct conversion [1]. The 48-V power bus reduces the current on power cables resulting in higher overall efficiency. It also reduces the system volume and is capable of delivering higher power. Therefore, with above superorities, direct 48–1-V point-of-load (POL) converters become essential and attractive in future systems.

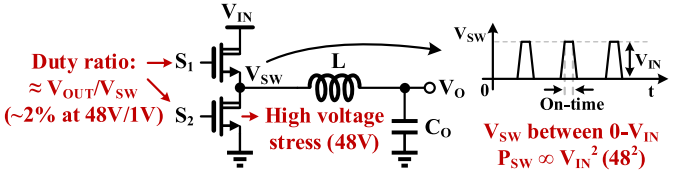

Fig. 1. Conventional half bridge topology at high-voltage conversion and its limitations.

However, efficient high-voltage conversion is not trivial. Fig. 1 shows an example of the conventional half bridge topology. First, the switching voltage (V_{SW}) of it trips between 0 V and the input voltage (V_{IN}). Such large voltage swing brings large switching loss (P_{SW}) which degrades the efficiency. Second, the duty ratio is close to the output voltage (V_O) over V_{SW} (around 2% for 48–1-V conversion). Such small duty ratio challenges control circuits, especially for high current designs that need to drive large devices. Finally, the high voltage stress (V_{STRESS}) requires high-voltage power switches which have large on-resistance (R_{ON}) and parasitic capacitance. Recent works of high-voltage half bridge converters all show low efficiency (<85%) or limited conversion ratios (<20) [2], [3], [4], [5], [6], [7]. To overcome the above issues, hybrid topologies are developed [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], and [20], [21] which combine switched capacitor circuits and inductors (Fig. 2). The key benefit of the hybrid topology is the reduced V_{SW} [22].

Therefore, it reduces P_{SW} and extends the duty ratio. Table I summarizes V_{SW} and duty ratios of recent hybrid converters. This work, considering the balance between area and efficiency, demonstrates a 0–4.8-V V_{SW} and a 20% duty ratio at 48–1-V conversion.

However, hybrid topologies still have limitations. First, they require large number of components, especially flying capacitors (C_{FS}). Usually, it requires N-1 C_{FS} for N times

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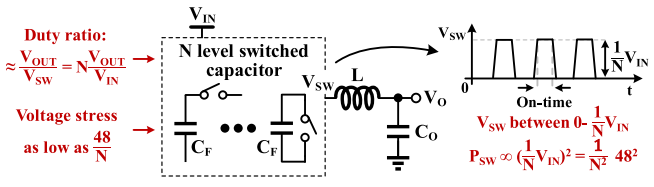


Fig. 2. Hybrid topologies overcoming the limitations in the half bridge topology.

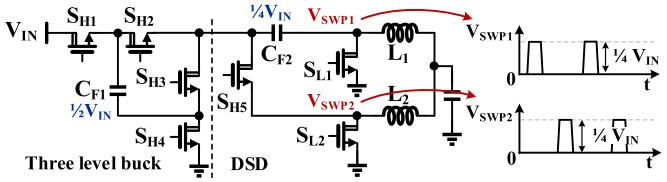


Fig. 3. Tri-state DSD topology [17] showing efficient C_F utilization.

TABLE I
SWITCHING VOLTAGES AND DUTY RATIOS OF 48–1-V CONVERTERS

	V_{SW}	Lowest voltage stress	duty ratio
Half bridge	0-48 V	48 V	2%
[12]	0-8 V	8 V	12.5%
[16]	0-6.8 V	6.8 V	14.2%
[18]	0-4 V	4 V	25%
This work	**0-4.8 V**	**4.8 V**	**20%**

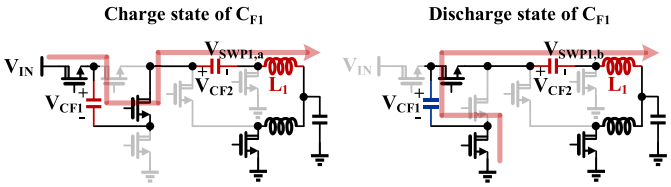


Fig. 4. C_{F1}-related operating states in tri-state DSD topology showing unbalanced C_{F1}.

V_{SW} reduction, similar to switched capacitor converters. As an example, [18] uses 11 C_Fs to reduce V_{SW} 12 times. Due to the low density of on-chip capacitors, most of the C_Fs are off-chip, which increases the area and cost. Second, as the power increases in data centers and other applications, the current range also increases [e.g., from 8–10 A (2-A range) to 80–100 A (20-A range)]. Although the power in data centers is mostly stable at the peak power, extending the operation range is required and beneficial if current variations exist. However, large power devices are required to reduce the conduction loss (P_{COND}) when the output current (I_O) is high, which brings large gate drive loss (P_G) as hybrid topologies require additional devices to bring down V_{SW}. P_G becomes dominant and reduces the efficiency when I_O is lower. Therefore, hybrid topologies have limited operation ranges (small I_O range at high efficiency) or they are not operating at the optimized condition across most of the current range. This work demonstrates a hybrid converter accomplishing direct 48–1-V conversion with high efficiency. Besides, this work reduces the number of off-chip C_Fs and optimizes the converter to achieve wide operation range, which overcomes the above limitations in hybrid topologies.

The rest of this article is organized as follows. The derivation and features of the proposed topology are discussed in Section II. Section III discusses the motivation, loss analysis, and the algorithm for the optimization. System architecture and circuit implementations are presented in Section IV. The experimental results are shown in Section V. Finally, Section VI concludes this work.

II. THREE-LEVEL HYBRID DICKSON TOPOLOGY

A. Topology Derivation and Operation

Fig. 3 shows a recent work of a tri-state double step-down (DSD) converter [17]. By combining the three-level buck topology and the DSD topology, its switching voltages (V_{SWP1} and V_{SWP2}) trip between 0 V and (1/4) V_{IN} with two C_Fs (Fig. 3). Intuitively, the three-level buck topology at the first stage brings down V_{IN} by half [10] and the reduced voltage becomes V_{IN} of the DSD topology. Next, the DSD topology brings down the voltage another half [8]. Such a two-stage hybrid converter shows a multiplication effect on voltage reduction, achieving an efficient utilization of C_Fs.

However, C_F self-balancing, which is inherent in the DSD topology, is not achieved in [17]. The second capacitor (C_{F2}) is balanced by two inductors (L_1 and L_2) as described in [8], but the first capacitor (C_{F1}) is unbalanced since it is not directly connected to inductors. Fig. 4 shows two operating states related to C_{F1}. The following two equations show switching voltages ($V_{SWP1,a}$ and $V_{SWP1,b}$) in these two states

$$V_{SWP1,a} = V_{IN} - V_{CF1} - V_{CF2} \quad (1a)$$

$$V_{SWP1,b} = V_{CF1} - V_{CF2}. \quad (1b)$$

From (1a) and (1b), no constrain exists for V_{CF1}, and the switching voltages in two states are not necessarily equal. Therefore, V_{CF1} can be any value depending on the initial condition, and C_{F1} is not self-balanced.

Inspired by [17], this work proposes a three-level hybrid Dickson topology achieving efficient C_F utilization and, more importantly, all C_Fs are self-balanced. Fig. 5 shows the proposed topology. Similarly, it has a three-level buck topology at first to bring down V_{IN} two times. In the next stage, the DSD stage is replaced by a five-level hybrid Dickson topology with four C_Fs. With the above modification, the proposed topology has the following benefits: 1) it brings down the switching voltages (V_{SWP1}–V_{SWP3}) ten times with only five C_Fs—a 45% reduction compared with the conventional hybrid topologies which requires nine C_Fs; 2) all C_Fs including C_{F1} are self-balanced; and 3) three inductors (L_1–L_3) form three-phase operation that is capable of delivering higher I_O and improves soft-charging between C_Fs compared with the conventional two-phase operation.

Fig. 6 shows the operating states of the proposed topology, including waveforms of switching voltages (V_{SWP1}–V_{SWP3}), voltages of C_Fs (V_{CF1}–V_{CF5}), and inductor currents (I_{L1}–I_{L3}). The converter operation is separated into six states. In each state, it has a charge phase that one of the inductors is charged and another discharge phase that all the inductors are discharged. In state one, L_1 is charged by V_{IN} and its current

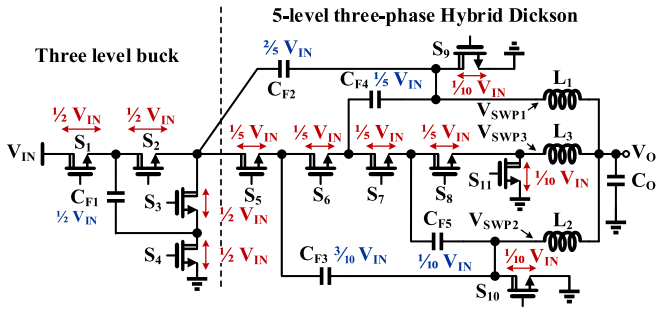


Fig. 5. Proposed three-level hybrid Dickson topology.

increases. During this time, V_{SWP1} increases to 4.8 V. Then all the inductors are discharged and V_{SWP1} decreases to 0 V. In state two, L_2 is charged by C_{F2}–C_{F5} and V_{SWP2} increases to 4.8 V. Then L_2 is discharged and V_{SWP2} becomes 0 V. In state three, L_3 is charged by C_{F5} only and V_{SWP3} increases to 4.8 V. Then L_3 is discharged and V_{SWP3} drops to 0 V. State one to state three form the first part of the operation consisting of half operation of the three-level buck topology [10] and full operation of the hybrid Dickson topology [12]. In state four, L_1 is charged again and C_{F1} provides current. V_{SWP1} increases to 4.8 V and then decreases to 0 V later. In state five, same as state two, L_2 is charged and V_{SWP2} increases to 4.8 V. Then L_2 is discharged. In state six, same as state three, L_3 is charged by C_{F5} and V_{SWP3} increases to 4.8 V. Finally, L_3 is discharged, and V_{SWP3} becomes 0 V. From waveforms in Fig. 6, first, the maximum voltages of V_{SWP1}–V_{SWP3} are all below 4.8 V, reducing P_{SW} and extending the duty ratio ten times. More importantly, only five C_Fs are used, overcoming the large number of C_Fs in the conventional hybrid topologies. Second, the proposed topology reduces V_{STRESS} on power switches. S_1–S_4 have 24-V V_{STRESS}, and S_5–S_8 have 9.6-V V_{STRESS}. S_9–S_{11} which are turned on most of the time only need to tolerate 4.8-V V_{STRESS}. Therefore, low-voltage Si devices can be used which provides high performance and dense integration. This also enables controls on power devices to optimize the efficiency, which cannot be implemented on off-chip Gallium Nitride (GaN) field-effect transistors (FETs). Finally, L_1–L_3 form three-phase operation with a 120° phase shift, and I_O is distributed among them by a ratio of 2:2:1, reducing the current stress on each inductor.

B. Flying Capacitor Self-Balancing

Balanced C_Fs are critical to the operation of hybrid converters. However, if C_Fs are not self-balanced, rebalancing techniques as presented in [17] are required, increasing the system complexity. C_F self-balancing is achieved in the proposed topology without any additional control. C_{F2}–C_{F5} are balanced by L_1–L_3 as described in [12] and [15] because they are connected to these inductors directly. Fig. 7 shows two operating states for C_{F1}. Switching voltages ($V_{SWP1,a}$ and $V_{SWP1,b}$) in two states can be described by (2)

$$V_{SWP1,a} = V_{IN} - V_{CF1} - V_{CF2} = V_{CF3} - V_{CF4} \quad (2a)$$

$$V_{SWP1,b} = V_{CF1} - V_{CF2} = V_{CF3} - V_{CF4}. \quad (2b)$$

$V_{CF3} - V_{CF4}$ appear in both the equations which represents the charging path of C_{F3} to C_{F4} in two states in Fig. 7. Therefore, $V_{SWP1,a}$ and $V_{SWP1,b}$ are equal to $V_{CF3} - V_{CF4}$. Then V_{CF1} can be described in the following equation:

$$V_{SWP1,a} = V_{SWP1,b} = V_{CF3} - V_{CF4} \quad (3a)$$

$$V_{IN} - V_{CF1} - V_{CF2} = V_{CF1} - V_{CF2} \quad (3b)$$

$$V_{CF1} = \frac{V_{IN}}{2}. \quad (3c)$$

Therefore, V_{CF1} is always half of V_{IN}. Although it is not connected to inductors directly, C_{F1} can be balanced by C_{F3} and C_{F4}. As a result, all C_Fs are self-balanced in the proposed topology, eliminating the rebalancing techniques.

C. Inductor Current Balancing

A converter with multiple inductors needs to ensure correct current sharing among inductors during the operation. The conventional multiphase converters require current-mode controls to balance inductor currents (I_Ls). However, accurate current-sensing or reconstruction at high frequency is challenging. In the proposed topology, I_Ls are balanced by C_Fs [8], [12], [21], which is highly advantageous. In the steady-state, according to the charge-second balance of C_F, the net charge (ΔQ) on each C_F in a cycle must be zero

$$\Delta Q = \int_{t_0}^{t_0+T} I_{CF}\, dt = 0. \quad (4)$$

Therefore, by keeping duty ratios equal in charging phases of all the operating states ($D_1 = D_2 = D_3$) shown in Fig. 6, the charging current ($I_{CF,a}$) and discharging current ($I_{CF,b}$) of each C_F are equal. For example, C_{F2} is charged in state 1.a and discharged in state 2.a

$$\Delta Q_{CF2} = \int_{t_0}^{t_0+T} I_{CF2}\, dt = I_{CF2,a} D_1 T - I_{CF2,b} D_2 T = 0$$
$$D_1 = D_2, \Rightarrow I_{CF2,a} = I_{CF2,b} = I_{CF2}. \quad (5)$$

Moreover, C_{F1} and C_{F2} are in series in state 1.a in Fig. 6, so $I_{CF1} = I_{CF2}$. Similarly, C_{F2} and C_{F3} are in series in state 2.a and $I_{CF2} = I_{CF3}$. C_{F3} and C_{F4} are in series in state 1.a, while C_{F4} and C_5 are in series in state 3.a. Therefore, all currents on C_Fs are equal

$$I_{CF1} = I_{CF2} = I_{CF3} = I_{CF4} = I_{CF5}. \quad (6)$$

Finally, from state 1.a, 2.a, and 3.a

$$I_{L1} = I_{CF1} + I_{CF3} = 2I_{CF1}$$
$$I_{L2} = I_{CF2} + I_{CF4} = 2I_{CF1}$$
$$I_{L3} = I_{CF5} = I_{CF1}. \quad (7)$$

Therefore, I_{L1}–I_{L3} are balanced to a ratio of 2:2:1 even with different inductances.

In turn, the charge-second balance of C_{F2} can be expressed by I_Ls

$$\int_{t_0}^{t_0+T} I_{CF2}\, dt = \frac{I_{L1}}{2} D_1 T - \frac{I_{L2}}{2} D_2 T = 0$$
$$D_1 = D_2, \Rightarrow I_{L1} = I_{L1}. \quad (8)$$

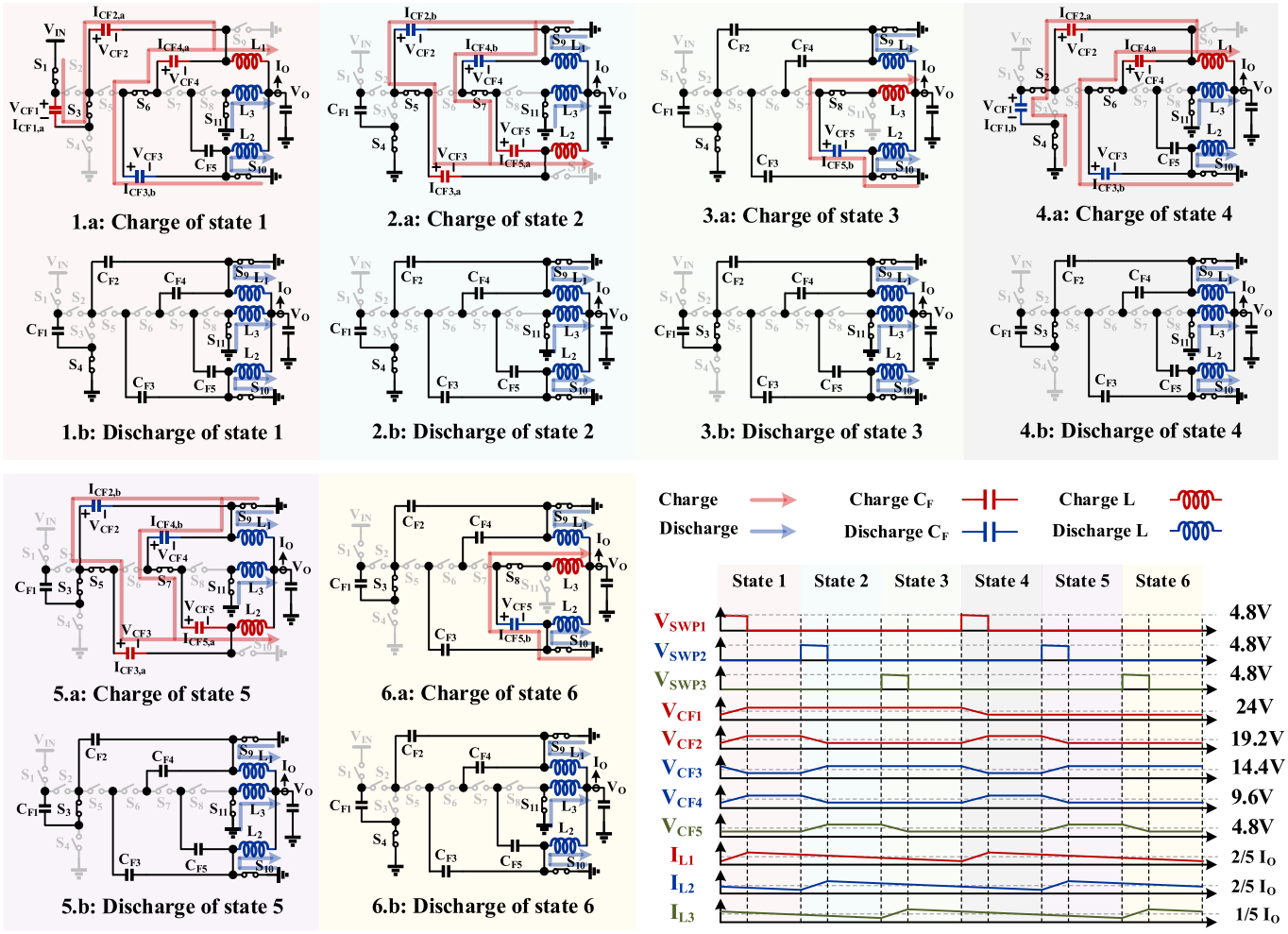


Fig. 6. Operating states and key waveforms of the proposed topology.

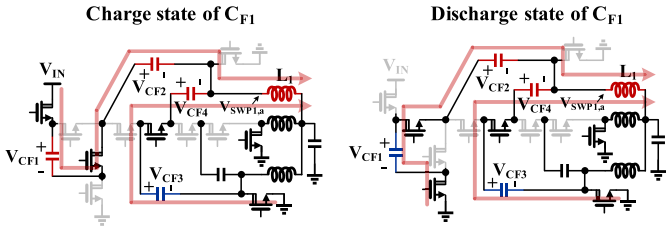


Fig. 7. C_{F1}-related operating states in the proposed topology showing C_{F1} self-balancing.

Similarly, for C_{F5}

$$\int_{t_0}^{t_0+T} I_{CF5}\,dt = \frac{I_{L2}}{2} D_2 T - I_{L3} D_3 T = 0$$
$$D_2 = D_3, \Rightarrow I_{L2} = 2\ I_{L3}. \tag{9}$$

Therefore, $I_{L1} = I_{L2} = 2I_{L3}$, as long as the charge-second balance holds and $D_1 = D_2 = D_3$.

Fig. 8 shows simulated I_Ls in different conditions. Fig. 8(a) shows the normal case that duty ratios and inductances are same. All I_Ls are balanced with the ratio of 2:2:1 as expected. In Fig. 8(b), the mismatch exists between duty ratios (D_1 = 0.9D, D_2 = D, and D_3 = 1.1D). Error exists among I_Ls. I_{L1} is higher than desired, while I_{L2} and I_{L3} are lower. Therefore, keeping duty ratios equal is important for balanced I_Ls. The current ripple (I_{ripple}) on L_3 is doubled when L_3 has half of the inductance compared with L_1 and L_2 as shown in Fig. 8(c). However, I_Ls still maintain the same DC values with Fig. 8(a). Fig. 8(d) shows when I_O changes, unbalancing occurs between I_Ls. However, by keeping $D_1 = D_2 = D_3$, all I_Ls will be balanced after some switching cycles. Therefore, the proposed topology achieves I_L self-balancing.

D. Soft-Charging Operation

Hard-charging occurs when a capacitor is connected to another capacitor or a voltage source with different voltages. Avoiding hard-charging reduces power loss and required capacitor size. However, without the split-phase control, the conventional odd-level Dickson structure faces hard-charging between C_Fs because of different number of charging paths [16], [23], [24]. Fig. 9(a) shows the same topology with only two inductors. When L_2 is charged, two capacitor paths (C_{F2} to C_{F3} and C_{F4} to C_{F5}) provide the current. After the charging phase of L_2, V_{CF2} and V_{CF4} drop ΔV, while V_{CF3} and V_{CF5} increase ΔV [Fig. 9(a)]. Where ΔV is the

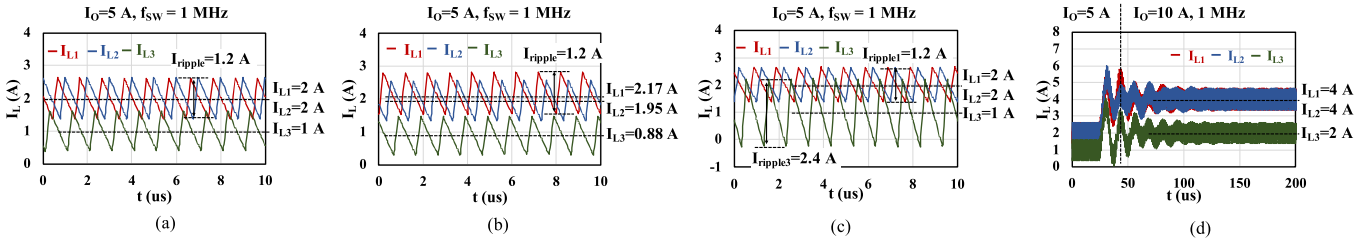


Fig. 8. Simulated inductor currents at different conditions: (a) $L_1 = L_2 = L_3 = 0.62\ \mu$H, $D_1 = D_2 = D_3 =$ D. (b) $L_1 = L_2 = L_3 = 0.62\ \mu$H, $D_1 = 0.9$D, $D_2 =$ D, $D_3 = 1.1$D. (c) $L_1 = L_2 = 0.62\ \mu$H, $L_3 = 0.31\ \mu$H, $D_1 = D_2 = D_3 =$ D. (d) $L_1 = L_2 = L_3 = 0.62\ \mu$H, $D_1 = D_2 = D_3 =$ D, with I_O step.

total voltage ripple of C_{F}s. In the next state when L_1 is charged, three capacitor paths (C_{F1} to C_{F2}, C_{F3} to C_{F4} and C_{F5}) provide the current [Fig. 9(b)]. According to the initial voltages on C_{F1}–C_{F5}, voltages of three capacitor paths at the beginning of this state can be described in Fig. 9(b). Since C_{F5} path has lower voltage (V_3) than the other two (V_1 and V_2), hard-charging occurs between C_{F}s at the beginning of the charging phase of L_1. To avoid hard-charging, this work adds another inductor L_3 to split C_{F5} out, forming a three-phase operation [15]. As shown in Fig. 9(c) and (d), charging of L_1 and L_2 involves two capacitor paths with the same voltage. Therefore, no C_{F5} path exists during the charging of L_1, which avoids hard-charging. Meanwhile, L_3 is charged by C_{F5} separately, forming the third operation phase [Fig. 9(e)]. With the three-phase operation, the proposed topology improves soft-charging and supports higher I_O compared with the two-phase topology.

III. Gradient Descent Optimization

To overcome limited operation ranges in the conventional hybrid topologies, a converter optimization is required. In this work, two parameters which optimize the efficiency are investigated. Fig. 10(a) shows the effect of switching frequency (f_{SW}) on the efficiency at different I_O. Optimal f_{SW} exists and it has a large dependence on I_O. The efficiency plot over f_{SW} also shows a convex curve. Fig. 10(b) shows loss distribution versus I_O. As I_O increases, $\mathrm{P_{COND}}$ becomes dominant. In order to maintain high efficiency, large power switches are required which bring high drive energy. However, if I_O is low, $\mathrm{P_G}$ of these large switches dominates. Since this work uses Si devices with customized sizes, turning on all the fingers of them wastes large amount of $\mathrm{P_G}$ but has very limited $\mathrm{P_{COND}}$ reduction. Therefore, adaptively choosing number of fingers (N_F) of Si devices based on I_O is necessary for optimized efficiency. It enables using large switches to reduce $\mathrm{P_{COND}}$ at heavy load but maintaining high efficiency at light load. Therefore, in this work, an optimization algorithm is proposed to find optimal f_{SW} and N_F of Si devices.

To find a proper algorithm, loss analysis of the converter is necessary. First, the effect of f_{SW} on converter's power loss ($\mathrm{P_{LOSS}}$) is investigated. For simplicity, $\mathrm{P_{LOSS}}$ can be divided into $\mathrm{P_{SW}}$, $\mathrm{P_G}$, and $\mathrm{P_{COND}}$. $\mathrm{P_{SW}}$ and $\mathrm{P_G}$ are proportional to f_{SW}, while $\mathrm{P_{COND}}$ is proportional to the normalized total resistance (R_{total}) as shown in the following equation:

$$P_{\mathrm{LOSS}} = \left(P_{\mathrm{SW},0} + P_{G,0}\right) f_{\mathrm{SW}} + I_{\mathrm{rms}}^2 R_{\mathrm{total}} \tag{10}$$

where $\mathrm{P_{SW,0}}$ is the normalized switching loss, $\mathrm{P_{G,0}}$ is the normalized gate drive loss, and I_{rms} is the root-mean-square (rms) value of the current. Considering I_{ripple} on the inductor which is inversely proportional to f_{SW}, I_{rms} can be estimated by the following equation:

$$I_{\mathrm{rms}} = \sqrt{I_O^2 + \frac{I_{\mathrm{ripple}}^2}{12}} = \sqrt{I_O^2 + \frac{I_{\mathrm{ripple},0}^2}{12 f_{\mathrm{SW}}^2}} \tag{11}$$

where $I_{\mathrm{ripple},0}$ is the normalized ripple current. Therefore, the total loss on the converter can be written in the following equation:

$$P_{\mathrm{LOSS}} = \left(P_{\mathrm{SW},0} + P_{G,0}\right) f_{\mathrm{SW}} + \left(I_O^2 + \frac{I_{\mathrm{ripple},0}^2}{12 f_{\mathrm{SW}}^2}\right) R_{\mathrm{total}}. \tag{12}$$

To find the optimal f_{SW}, take the derivative of $\mathrm{P_{LOSS}}$ and set it to zero

$$P'_{\mathrm{LOSS}} = P_{\mathrm{SW},0} + P_{G,0} - \frac{I_{\mathrm{ripple},0}^2 R_{\mathrm{total}}}{6 f_{\mathrm{SW}}^3} = 0. \tag{13}$$

Therefore, the optimal f_{SW} can be estimated as

$$f_{\mathrm{SW,OPT}} = \sqrt[3]{\frac{I_{\mathrm{ripple},0}^2 R_{\mathrm{total}}}{6\left(P_{\mathrm{SW},0} + P_{G,0}\right)}}. \tag{14}$$

From (14), when R_{total} is small which means large devices are used, f_{SW} is low to reduce $\mathrm{P_{SW}}$ and $\mathrm{P_G}$. The above analysis is consistent with the simulation in Fig. 10(a).

Next, the relationship between N_F and the loss on the power switch ($\mathrm{P_{SWITCH}}$) is investigated. Fig. 11 shows a simplified switch model. The switch is modeled as its R_{ON} with its gate capacitor (C_{G}) and drain capacitor (C_{DS}). Their relations to N_F can be described by the following equations:

$$R_{\mathrm{ON}} = \frac{R_{\mathrm{ON},0}}{N_F} \tag{15a}$$

$$C_G = C_{G,0} N_F \tag{15b}$$

$$C_{\mathrm{DS}} = C_{\mathrm{DS},0} N_F \tag{15c}$$

where $R_{\mathrm{ON},0}$, $C_{\mathrm{G},0}$, and $C_{\mathrm{DS},0}$ are the unit on-resistance, gate capacitor, and drain capacitor of the switch, respectively. The main loss on the switch can be divided into three parts. First, each time the switch is turned on, its C_{G} needs to be charged. Then C_{G} is discharged to turn off the switch, which leads to $\mathrm{P_G}$

$$P_G = V_G^2 C_{G,0} N_F f_{\mathrm{SW}} \tag{16}$$

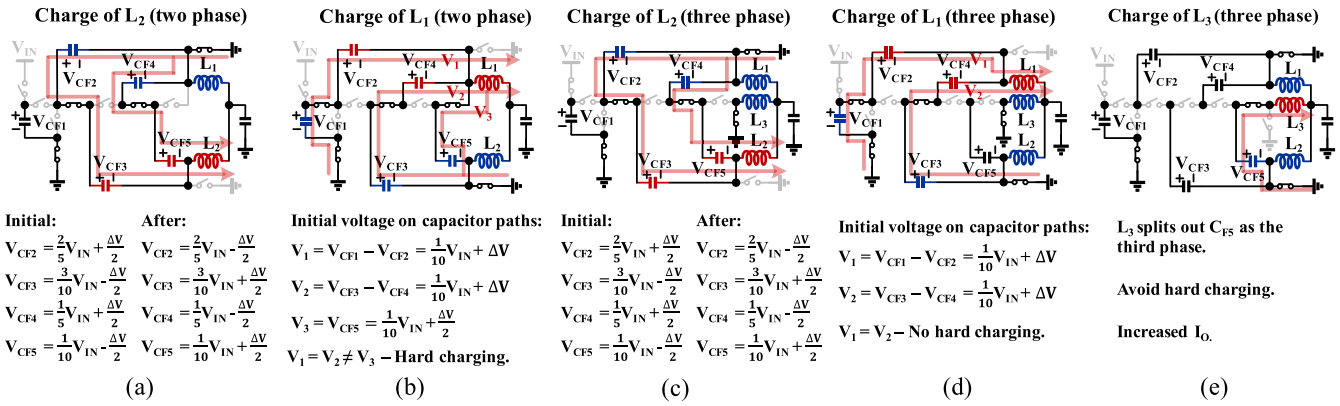


Fig. 9. Charge of (a) L_2 in the two-phase topology, (b) L_1 in the two-phase topology showing hard-charging, (c) L_2 in the three-phase topology, and (d) L_1 in the three-phase topology avoids hard-charging. (e) Third phase splits C_{F5} in the three-phase topology.

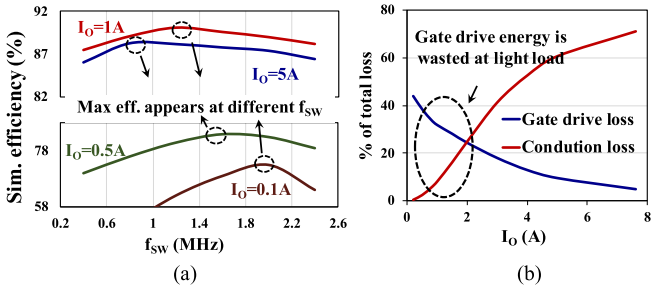


Fig. 10. (a) Simulated efficiency over f_{SW} at different I_O. (b) Loss distribution of P_G and P_{COND} over I_O.

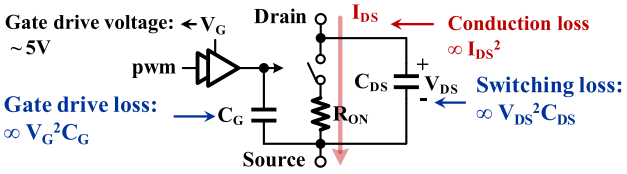


Fig. 11. Circuit model of a power switch.

where V_G is the drive voltage of the switch, typically 5 V. Second, C_{DS} brings P_{SW} (17) since it is charged and discharged by the drain–source voltage (V_{DS}) in every cycle

$$P_{SW} = \frac{1}{2} V_{DS,MAX}^2 C_{DS,0} N_{F,MAX} f_{SW} \tag{17}$$

where $V_{DS,MAX}$ is the maximum drain–source voltage on the switch, and $N_{F,MAX}$ is the maximum number of fingers of the switch. Although part of fingers are not turned on, the total C_{DS} still needs to be charged. Therefore, P_{SW} does not change with N_F. Finally, the switch has P_{COND} (18) which is proportional to its R_{ON}

$$P_{COND} = I_{DS}^2 \frac{R_{ON,0}}{N_F} \tag{18}$$

where I_{DS} is the rms current through the switch. Combining the above three main losses on the switch, it gives a loss equation for P_{SWITCH}

$$\begin{aligned} P_{SWITCH} &= P_G + P_{SW} + P_{COND} \\ &= V_G^2 C_{G,0} N_F f_{SW} + \frac{1}{2} V_{DS,MAX}^2 C_{DS,0} N_{F,MAX} f_{SW} \\ &\quad + I_{DS}^2 \frac{R_{ON,0}}{N_F}. \end{aligned} \tag{19}$$

When N_F increases, it reduces P_{COND} but increases P_G. Therefore, an optimal N_F exists which gives a balanced loss distribution on a switch. To obtain the minimum loss on the switch, take the derivative of (19) over N_F and set it to zero

$$P'_{SWITCH} = V_G^2 C_{G,0} f_{SW} - I_{DS}^2 \frac{R_{ON,0}}{N_F^2} = 0. \tag{20}$$

The optimal N_F under certain f_{SW} and I_{DS} is given by the following equation:

$$N_{F,OPT} = \sqrt{\frac{I_{DS}^2 R_{ON,0}}{V_G^2 C_{G,0} f_{SW}}}. \tag{21}$$

From (21), when I_{DS} is small which means I_O is low, only part of fingers should be turned on to save drive energy. On the contrary, high I_O requires more fingers to be turned on, showing a tradeoff between P_{COND} and P_G. Although different switches have different losses (S_3–S_8 have large P_{SW} which dominates when I_O is low, while S_9–S_{11} have large P_{COND} which dominates when I_O is high), optimizing both high-side and low-side switches are beneficial since it reduces unnecessary P_G.

The above analysis shows the loss of the converter over f_{SW} and the loss of the switch over N_F. It gives equations for optimal f_{SW} and N_F. However, directly calculating $f_{SW,OPT}$ and $N_{F,OPT}$ is not accurate because of parasitics and identifying I_{DS} for each switch involves the challenging high-voltage current-sensing. Therefore, since P_{LOSS} and P_{SWITCH} are convex functions, a simple gradient descent method can find $f_{SW,OPT}$ and $N_{F,OPT}$ efficiently. By comparing P_{LOSS} in each step, it tunes f_{SW} and N_F until the gradient is positive, which is implemented in Section IV.

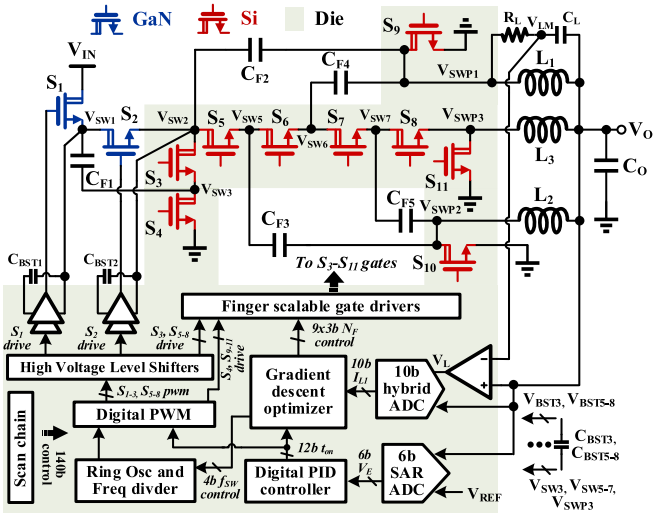


Fig. 12. System architecture of the proposed high-voltage converter.

TABLE II
OFF-CHIP COMPONENTS' LIST

Component	Value
S_1, S_2	65 V GaN [25]
L_1 – L_3	0.62 μH
C_{F1} – C_{F5}	1 μF
C_{BSTX}	0.1 μF
C_O	10 μF

TABLE III
POWER SWITCH LIST

Device	Type	*R_{ON}·Q_{OSS} (mΩ·nC)	*R_{ON}·Q_G (mΩ·nC)	Unit width x Finger
S_1, S_2	65 V GaN	84.6	33.3	/
S_3 – S_4	24 V Si	37.4	67.2	5 mm x 8
S_5	24 V Si	37.4	67.2	7.8 mm x 8
S_6	20 V Si	25.7	47	7.08 mm x 8
S_7	16 V Si	16.1	42	6 mm x 8
S_8	12 V Si	9.4	25.67	5 mm x 8
S_9 – S_{10}	6 V Si	4.4	16.18	12 mm x 8
S_{11}	6 V Si	4.4	16.18	9 mm x 8

*number estimated from datasheet and simulation in 0.18 μm BCD process.

IV. SYSTEM ARCHITECTURE AND CIRCUIT IMPLEMENTATIONS

A. Converter System

Fig. 12 shows the system architecture of this work. The colored area indicates the die. On top of it, the proposed three-level hybrid Dickson topology is shown. The off-chip components and power switches are shown in Tables II and III. Since the floating-substrate process is not available for high-voltage Si devices in the used technology [0.18-μm Bipolar-CMOS-DMOS (BCD)], the substrate of these devices is always connected to the ground. Although S_1 and S_2 only need to withstand 24 V as shown in Fig. 5, their max drain-to-substrate voltages are 48 V when S_1 is turned on. Thus, 48-V devices are required for S_1 and S_2. However, Si devices have low density and large resistance at such high voltage, which occupies large chip area and lowers the efficiency. Therefore, off-chip GaN FETs [25] which have better performance are used for S_1 and S_2. S_3–S_{11} have lower stress (<24 V) on their drain-to-substrate voltages, so they are Si devices on the die as shown in Table III. According to their drain-to-substrate voltages, different devices are used to optimize the efficiency. This forms a GaN/Si hybrid conversion that reduces off-chip switches and improves the power density [18]. Si devices with customized fingers also enable proposed optimization algorithm in Section III. If the floating-substrate process is available, 24-V Si devices can be used for S_1–S_2 and 12-V Si devices can be used for S_3–S_8. Although L_3 carries less current than L_1 and L_2, using a smaller inductor for L_3 increases I_{ripple} on it as shown in Fig. 8(c), which is not desired. To avoid the mismatch, unequal I_{ripple}s, and the complexity (different footprints and materials), the same inductors for L_1–L_3 are used [16].

In the control chip, first, it has a regulation loop to accomplish converter's operation. It senses V_O by a 6-bit successive-approximation analog-to-digital converter (SAR ADC). Then the error voltage (V_E) is sent to a programmable digital proportional–integral–differential (PID) controller, which calculates the 12-bit on-time (t_{ON}). Based on t_{ON}, the digital pulsewidth modulator (PWM) generates gate signals with a resolution of 156 ps and the switching clock is generated from a ring oscillator. Since source terminals of S_1–S_3, and S_5–S_8 are floating, gate signals of them are first sent to high-voltage floating level shifters supplied by 0.1 μF off-chip bootstrap (BST) capacitors (C_{BST1}–C_{BST3}, C_{BST5}–C_{BST8}) to accomplish high-voltage gate driving. GaN switches (S_1 and S_2) use single gate drivers, and Si switches (S_3–S_{11}) are driven by finger scalable gate drivers which are capable of 3-bit N_F tuning. Second, a optimization loop is implemented to dynamically tune f_{SW} and N_F during the converter's operation. To have a precise power loss estimation, a filter-based current sensor with an differential amplifier is used to sense L_1's average current (I_{L1}). Then the sensed voltage (V_L) is converted by a 10-bit hybrid ADC. The 10-bit I_{L1} along with the 12-bit t_{ON} are sent to a gradient descent run-time optimizer. The optimizer calculates the power loss at each gradient descent step and compares them to find the optimal f_{SW} and N_F. f_{SW} is controlled by a ring oscillator with a frequency divider capable of 4-bit frequency tuning. The 9 × 3-bit N_F of S_3–S_{11} are sent to finger scalable gate drivers to drive Si switches.

B. Circuit Implementations

In high-voltage converters, level shifters are critical for successful gate driving. However, to ensure reliability during high dV/dt conditions, the conventional level shifter uses four cascoded high-voltage devices which brings large area and slow speed [26], [27]. The proposed high-speed digital-assisted level shifter is shown in Fig. 13. To avoid the static power, a short pulse generator generates pulses (<2 ns) from edges of the input to IN_P (rising edge) and IN_N (falling edge). Only two high-voltage devices (M_{H1} and M_{H2}) are used which reduces the area, and diode clamped transistors (M_1 and M_2) improve

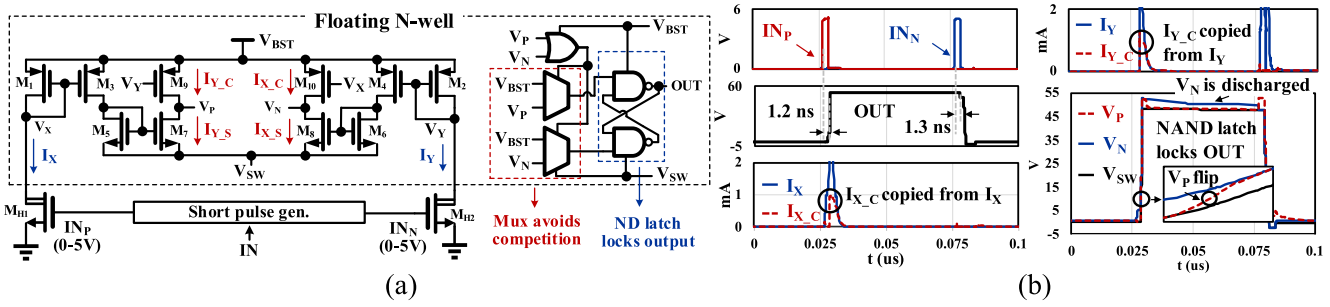


Fig. 13. (a) Proposed high-reliability digital-assisted high-voltage floating level shifter. (b) Simulation waveforms showing improved reliability.

the speed [27]. Current mirrors (M_3–M_{10}) provide symmetric pull-up and pull-down time. To improve the reliability, a digital logic has been added in the same floating N-well ($V_{DD} = V_{BST}$, $V_{SS} = V_{SW}$) with the level shifter. During the rising time when V_{SW} increases, large transient current I_{X_C} and I_{Y_C} copied from I_X and I_Y by current mirrors charge V_P and V_N nodes to high [Fig. 13(b)]. To avoid output flipping, a NAND latch is used to lock the output when both the inputs are high. During the steady-state, small static current I_{X_S} and I_{Y_S} continuously discharge V_P and V_N making inputs of NAND latch both low [Fig. 13(b)]. To avoid competitions between digital cells, two 2-to-1 Muxes with an OR gate are used to block both low inputs to the NAND latch. From the simulation shown in Fig. 13(b), the output of the level shifter is correct during high dV/dt conditions (80 V/ns). With small digital cells, compared with the conventional cascoded level shifter, the proposed design shows high speed (<1.5 ns), small area (200 × 65 μm) and high reliability.

To implement the gradient descent algorithm, the knowledge of P_{LOSS} is required which can be estimated by the input current (I_{IN}). However, directly sensing I_{IN} is hard because: (1) I_{IN} is small (mA), and adding high-resistance path to sense it lowers the efficiency significantly. (2) I_{IN} is in the high-voltage region, increasing the complexity of sensing circuits. Therefore, this work senses I_{L1} instead as an estimation, which contains I_{IN} when S_1 is turned on. The current-sensing circuit is shown in Fig. 14. It uses a filter-based current sensor (C_L and R_L) as the front-end. With proper component selection ($R_L C_L = (L/\text{DCR})$), the voltage across C_L will be proportional to I_{L1}. Where DCR is the inductor DC resistance. This method eliminates the sensing resistor which brings substantial loss. Next, V_{LM} and V_O are sent to a differential amplifier shown in Fig. 14. Since only average I_{L1} is required, the folded cascode structure is used to provide high gain and its bandwidth is set low to filter out high-frequency noise. The gain of the differential amplifier (R_4/R_1) is set to (1/2DCR). Then, V_L which indicates I_{L1} is converted by an ADC. Considering the available area and design complexity, a 10-bit ADC is used. To reduce power and area overhead of the ADC, Fig. 14 shows the proposed 10-bit hybrid ADC. It has a capacitor-based 5-bit SAR ADC in the front which converts the first 5 bits of V_L (I_{L1}[9:5]). After the conversion, small residual voltages (V_{RES1} and V_{RES2}) are stored on capacitors in the SAR ADC. The second part of the ADC is a 5-bit time-domain ADC consisting of voltage-to-time converters (VTCs), a time-to-digital converter (TDC), and a thermometer-to-binary converter. V_{RES1} and V_{RES2} are directly sent to tail transistors (M_T) of two VTCs. At the meantime, the SAR register will send a pulse (P) to both the input inverters of VTCs. The voltage difference between V_{RES1} and V_{RES2} is converted into time difference between P_1 and P_2. Since the difference between V_{RES1} and V_{RES2} is small (<62.5 mV), current-controlled inverters in VTCs show good linearity. Then, P_1 and P_2 are sent to delay lines in TDC with 1-ns delay difference between delay cells. Outputs of P_1 or P_2 delay cells are connected to data ports or clock ports of flip-flops, respectively. Since P_1's rising edge is faster than P_2 at first, outputs of flip-flops are high. After certain amount of delay cells, the rising edge of P_1 is after that of P_2, and the outputs of the remaining flip-flops become low. Depending on the time difference between P_1 and P_2, the number of flip-flops that output high changes, showing the time-to-digital conversion. A total of 32 flip-flops are used to achieve 5-bit resolution. Finally, a thermometer to binary converter converts the later 5 bits of V_L (I_{L1}[4:0]), completing the 10-bit conversion. The proposed two-stage hybrid ADC only uses a 5-bit SAR ADC which has 32x less capacitor area than a 10-bit SAR ADC. Compared with a conventional integral ADC, the proposed design eliminates the intermediate amplifier by reusing voltages on capacitors and uses the time-domain ADC to maintain good linearity, showing 20% reduced power consumption. Therefore, the proposed design accomplishes 10-bit conversion with small area and power.

Fig. 15 shows the optimization circuit. I_{L1} is sent to a power loss calculator after a 4-bit manual offset calibration ($I_{L1,CAL}$[3:0]) to estimate P_{LOSS}. The equation of P_{LOSS} is shown on the left. To accurately estimate the input power (P_{IN}), it uses half of I_{L1} to estimate the average I_{IN} and t_{ON} from the PID controller for turn-on time of S_1. The estimation of unit drive loss ($P_{G,0}$) is based on the simulation including parasitics. Since f_{SW} and N_F are correlated, an iterative gradient descent method is used. The outer loop optimizes f_{SW} and the inner loop optimizes N_F. At each step of f_{SW}, N_F is optimized to find the optimal efficiency at this f_{SW}. Starting from the smallest f_{SW}, it fixes f_{SW} and optimizes N_F. After each change in N_F, the current sensor senses I_{L1}. To ensure accurate current-sensing, the hybrid ADC starts the conversion after PID controller is stabilized. Then, the power

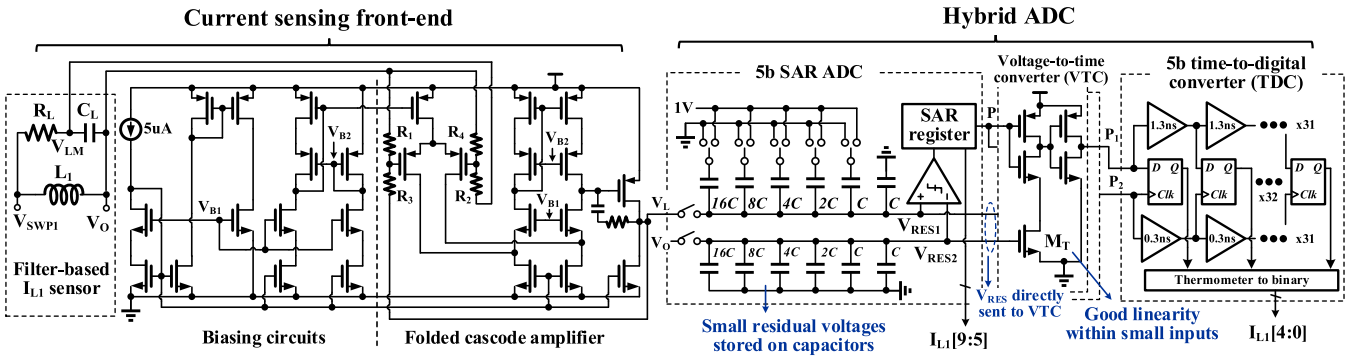


Fig. 14. Proposed current-sensing circuit with hybrid ADC achieving small area and power.

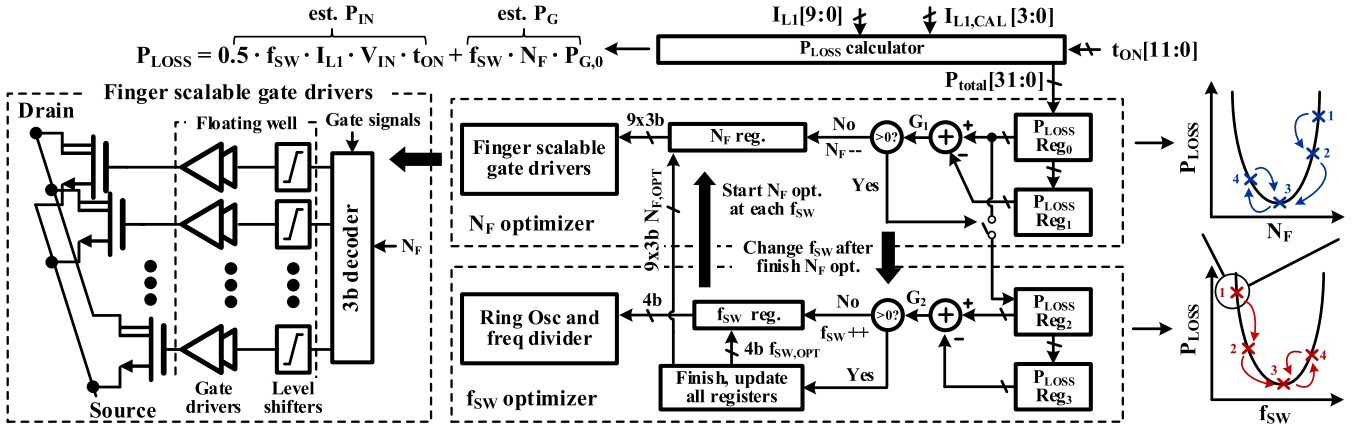
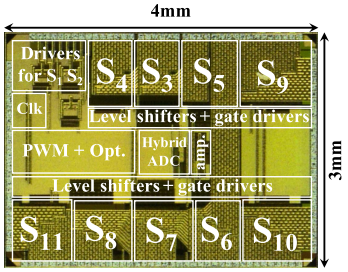


Fig. 15. Circuit diagram of the proposed digital gradient descent optimization method for f_{SW} and N_F.

loss calculator estimates P_{LOSS} and stores P_{LOSS} to the register (Reg_0). The N_F optimizer calculates the gradient (G_1) from registers (Reg_0 and Reg_1) each step. If G_1 is negative, which means P_{LOSS} decreases, N_F is subtracted by one, and the new P_{LOSS} is sensed and calculated again. If G_1 is positive, which means P_{LOSS} increases, N_F optimization is finished for this f_{SW} and P_{LOSS} is sent to the register in the f_{SW} optimizer (Reg_2). The f_{SW} optimizer calculates the gradient (G_2) after N_F optimization for this f_{SW} is completed. If G_2 is negative, f_{SW} is added and N_F is optimized again at the new f_{SW}. If G_2 is positive, the whole optimization is finished. The stored $N_{F,OPT}$ and $f_{SW,OPT}$ are sent to gate drivers and the frequency divider, respectively. The finger scalable gate drivers are shown in Fig. 15. For each power switch, it consists of a 3-bit decoder and arrays of gate drive stages. According to N_F, the gate signal is only sent to required drive stages to drive proper fingers of the power switch. Other outputs of the decoder are kept low. Using the above method, the run-time optimizer finds the global optimum for both f_{SW} and N_F during converter's operation.

V. Measurement Results

The test chip is fabricated in a 0.18-μm BCD process with an area of 4 × 3 mm^2. The chip die shot and characteristics are shown in Fig. 16. The converter board is shown in Fig. 17. By reducing off-chip C_Fs and switches, the power stage (switches, inductors, and C_Fs) of this work occupies



Technology	180nm HV BCD
Die Area	4 mm x 3 mm
Core V_{DD}	5 V
Package	Chip on board

Fig. 16. Chip die shot and characters.

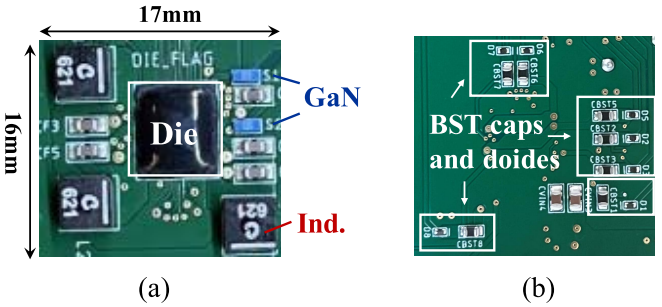


Fig. 17. Converter board photographs. (a) Top side (power stage). (b) Back side (BST circuits).

an area of 17 × 16 mm^2. It only has one side of components [Fig. 17(a)], reducing the height of the converter to only 3 mm. BST capacitors (C_{BST1}–C_{BST3}, C_{BST5}–C_{BST8}) and diodes are off-chip on the back side of the board shown in Fig. 17(b).

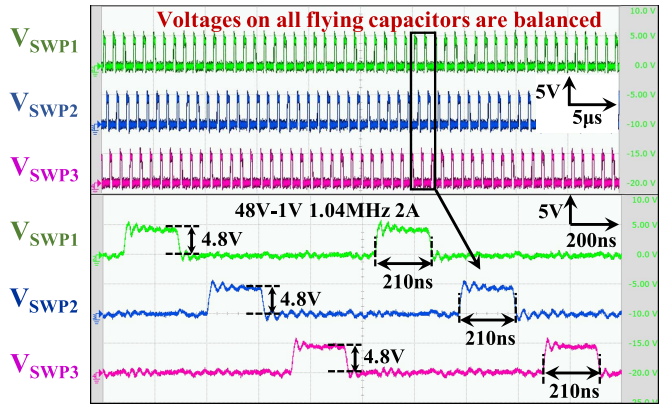


Fig. 18. Measured switching voltages showing 10x voltage reduction and flying capacitor self-balancing.

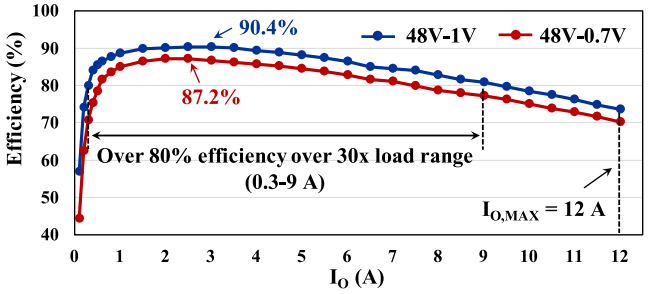


Fig. 19. Measured efficiency at 48–1- and 48–0.7-V conversion.

During the startup, the converter is first turned on at 5-V V_{IN} to avoid large voltage spike. Then, V_{IN} is slowly increased to 48 V. Due to the self-balancing feature of the topology, V_{CF}s and I_Ls are always balanced during the process. Fig. 18 shows measured switching waveforms. All the three switching voltages (V_{SWP1}–V_{SWP3}) trip between 0 and 4.8 V with a phase shift of 120°, validating the proposed topology. The duty ratio is around 20% and t_{ON} is over 200 ns at 1 MHz f_{SW}, relaxing the timing requirement. In a larger timescale, V_{SWP1}–V_{SWP3} are all stable and constant, which indicates that voltages on all C_Fs are balanced. The measured efficiency is shown in Fig. 19. By reducing V_{SW}, this work achieves 90.4% and 87.2% peak efficiency at 48–1- and 48–0.7-V conversions, respectively. The third phase L_3 pushes the maximum I_O to 12 A—50% higher than [18] which has two inductors. With the proposed optimization, the efficiency is over 80% for a 30x load range (0.3–9 A), showing a wide operation range.

Figs. 20 and 21 show efficiency improvements with the proposed gradient descent run-time optimizer. Fig. 20 shows comparison with 1 MHz f_{SW}. At light load (I_O = 0.1 A), the proposed method saves large amount of the drive energy. Compared with the non-optimized condition (N_F = 8 and f_{SW} = 1 MHz), the efficiency is improved by 16.9%. Although the efficiency is still below 60%, such load condition rarely happens in the practical usage when the designed max I_O is over 10 A. A more common case is I_O = 1 A, where the efficiency is improve by 3%. As I_O increases, the efficiency improvement decreases because P_{COND} overwhelms

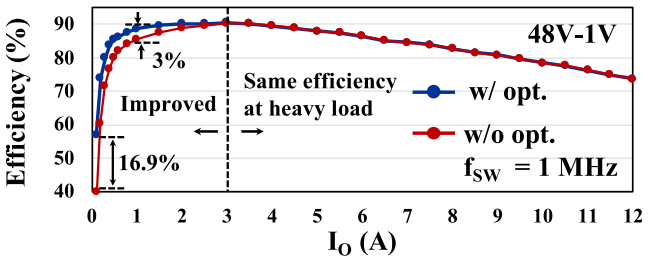


Fig. 20. Measured efficiency improvement with the proposed optimization at 48–1-V compared with normal operation (f_{SW} = 1 MHz, N_F = 8).

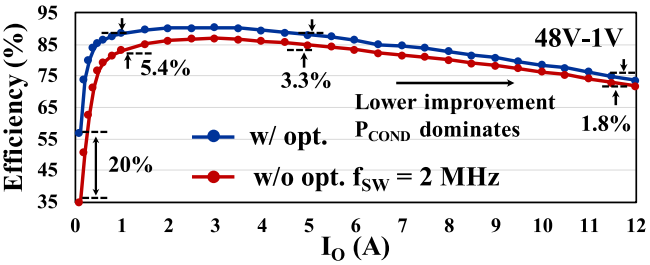


Fig. 21. Measured efficiency improvement with the proposed optimization at 48–1 V compared with normal operation (f_{SW} = 2 MHz, N_F = 8).

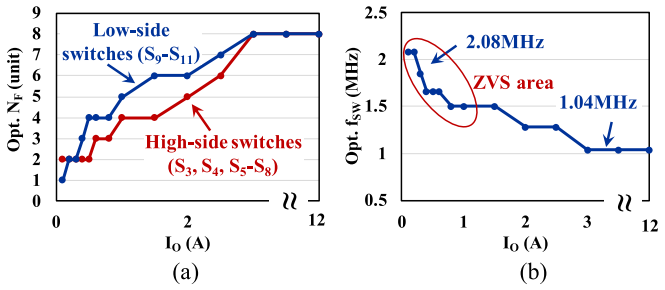


Fig. 22. (a) Measured optimal N_F over I_O. (b) Measured optimal f_{SW} over I_O.

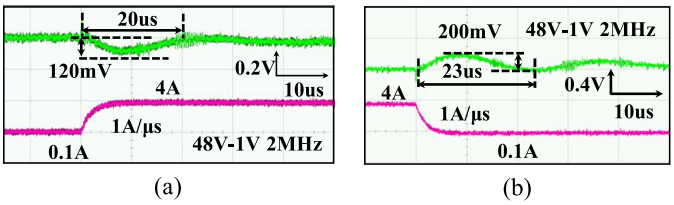


Fig. 23. (a) Measured low-to-high step response. (b) Measured high-to-low step response.

other losses. In Fig. 21, since all the fingers are turned on and f_{SW} is 2 MHz, large P_G reduces the efficiency to below 40% at light load. With optimization, the efficiency is improved over 20%. Since 2 MHz is not the optimized f_{SW}, the efficiency is improved over a wide range of I_O (5.4% at 1 A, 3.3% at 5 A). However, when I_O becomes higher, lower improvement is observed because P_{COND} dominates.

Fig. 22(a) shows measured optimal N_F at different I_O. As expected, N_F is small at light load to save drive energy. As I_O increases, N_F increases and finally reaches the maximum when I_O is higher than 3 A. N_F of low-side switches

TABLE IV
COMPARISON WITH THE STATE-OF-THE ART

	[12]	[17]	[9]	[18]	**This work**
Technology	Discrete	0.18 μm BCD	0.18 μm BCD	0.18 μm BCD	**0.18 μm BCD**
Topology	Dual-phase dual-inductor	Tri-state double-step down	Double-step down	12-level series-capacitor	**3-level hybrid Dickson**
V_{IN}	48-54 V	12/24 V	48 V	36-60 V	**48 V**
V_O	1-2 V	1 V	1 V	0.5-1 V	**0.7-1 V**
$I_{O,MAX}$	10 A	3 A	1.5 A	8 A	**12 A**
Power switches	External GaN	On-chip Si	External GaN	On-chip Si + External GaN	**On-chip Si + External GaN**
Inductor	2 x 1.5 μH	2 x 0.56 μH	2 x 0.9 μH	2 x 0.1 μH	**3 x 0.62 μH**
Number of C_Fs	5	2	1	11	**5**
Voltage reduction	6x	4x	2x	12x	**10x**
Number of external switches	8	0	4	1	**2**
Peak efficiency	95.02%@48-2 V 300 KHz	88.3%@24-1 V 100 KHz	85.4%@48-1 V 100 KHz	90.2%@48-1 V 2.5 MHz	**90.4%@48-1 V 1 MHz**
On-chip optimization	No	No	No	No	**Yes**
Current density	112.5 A/in^3	/	/	196/*998 A/in^3	**#240/#*992 A/in^3**

*Components volume only. #Exclude BST capacitors.

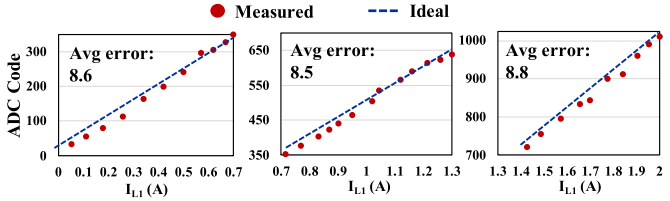


Fig. 24. Measured current-sensing error.

(S_9–S_{11}) is higher than that of high-side switches (S_3–S_8) because S_9–S_{11} conduct most of the current. Optimal f_{SW} versus I_O is shown in Fig. 22(b). At low I_O, switches are zero-voltage-switched (ZVS) reducing most of P_{SW}. Since N_F is low, P_G is kept small. Therefore, both P_{SW} and P_G are not increasing with f_{SW} significantly. To reduce I_{ripple} which dominates P_{COND} when I_O is low, f_{SW} is tuned higher. As I_O increases, more fingers are turned on to reduce P_{COND} and it is out of the ZVS region. f_{SW} is reduced to keep P_{SW} and P_G small. The measured step response is shown in Fig. 23. The 120-mV voltage drop and 20 μs response time are measured at a load step of 1 A/μs [Fig. 23(a)]. The 200-mV voltage overshoot and 23-μs response time are measured at the same high-to-low load step [Fig. 23(b)]. Fig. 24 shows measured current-sensing accuracy with the proposed hybrid ADC. It shows good linearity with a resolution of 2 mA. Since optimization is not required at heavy load, the maximum current-sensing range is 2 A ($I_O \approx 5$ A). The average error of sensing is around 8.5. The main sources of the error are from amplifier noise, V_O noise, and ADC nonlinearity. Although sensed I_{L1} has error, optimization only considers the difference between two steps. Therefore, the current-sensing circuit meets the requirement.

Table IV shows the comparison with the state-of-the-art. With the proposed topology, this work achieves high-voltage step-down conversion. Ten times voltage reduction is achieved with only five C_Fs, which shows the most efficient utilization of C_Fs. It achieves the highest efficiency (90.4%) among non-isolated 48–1-V converters operating at the MHz range. To the best of authors' knowledge, this work presents the first on-chip run-time optimization for non-isolated 48–1-V converters. Finally, by reducing the number of C_Fs and using GaN/Si hybrid conversion, this work achieves high current density.

VI. CONCLUSION

This article presents a direct 48–1-V DC–DC POL converter with a novel three-level hybrid Dickson topology, which overcomes the limitations in the conventional hybrid topologies. It accomplishes high-voltage step-down conversion with high peak efficiency (90.4%), high f_{SW} (>1 MHz), and high current density (992 A/in^3). The proposed topology reduces the number of C_Fs required to bring down the voltage in the conventional hybrid topologies, reducing the cost and size. Moreover, it also shows how all C_Fs can be self-balanced in a two-stage-like hybrid converter. In this work, GaN/Si hybrid conversion not only improves the power density but also enables using digital optimization on power devices. With the proposed run-time optimization, large devices can be used to achieve high I_O, but still maintain the efficiency as high as possible when I_O is lower, which is always beneficial. In the control chip, a hybrid ADC design is proposed completing data conversion for accurate current-sensing with small area and power overhead. In conclusion, this work presents an optimized design considering efficiency, the number of components, power density and operation range.

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