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A low power and PVT variation tolerant mux-latch for serializer interface and on-chip serial link

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ABSTRACT

Multiplexer (mux) latch is one of the key components for serializer interface to admit communication at Gbps. This work describes the working of a 2:1 mux-latch coupled to a power delivery network (PDN) and a CPU core drawing abrupt current. In comparison to conventional designs, multiplexer and latch operate at the same time, which is quite different because enable inputs are imperative to start latch operation. An analytical model is also derived to understand power delay trade-off and to choose gate sizes to obtain a comparable delay without increasing power. The average power and delay in post-layout are 257.7 μW and 35 ps, respectively, in a 90-nm CMOS, power supply voltage (Vdd) of 1.1 V and a clock switching at 6.25 GHz. However, a 117^{O}C change in temperature at distinct corner allows average power to vary between 32.8 and 64 μW. The corresponding variation is 135–183.7 μW as Vdd switches from 0.75 to 1.1 V. In addition to so, delay changes between 5-14 ps and 3–12 ps for the given change in temperature and Vdd, respectively. Nonetheless, the effective supply voltage V_P oscillates with time as the CPU core draws abrupt current. The delay values due to AC noise are found to be different than V_P having no noise and the corresponding jitter changes linearly as a function of noise.

1. Introduction

Serial link transceiver with serializer (Ser) and deserializer (Des) are essential to allow communication between on-chip cores and different building blocks operating at Gbps [1], Fig. 1. In addition to so, wireless and wireline communication require SerDes to be integrated on a single chip to admit transmission at Gbps. However, the performance of a serial link transceiver in terms of power and layout area depends on the design of a SerDes [2,3]. Following this, the present work describes the working of a multiplexer-latch, a fundamental block to design a power efficient serializer. Multiplexer-latch also referred to as mux-latch is used not only to convert parallel data into serial datum but also to retain its logic level before being fed into next stage [4]. Typically, CMOS process is preferred to design a mux-latch, but the system current increases linearly with operating frequency [5,6]. Since low power is a desired feature, current mode logic (CML) is chosen to maintain a constant system current with increasing operating frequency in each process [7,8]. Further, CML and its improvement are preferred to design mux-latch to operate at less than 1.5 V power supply voltage (Vdd) and high frequency [9]. To achieve this, CML designs are modified to accommodate additional gates, which in turn require bias circuitry to generate bias voltage. Additional gates and bias circuit maintain an almost full voltage swing, power-delay trade-off, but at the cost of layout area. Another effective way to minimize power dissipation is to reduce the operating voltage Vdd because power is proportional to square of Vdd. But CMOS process allows threshold voltage to decrease as well and affects the noise tolerance of a circuit because noise does not scale down proportionally with Vdd [10]. Therefore, it is imperative to understand noise margin in low power and deep submicron design. Besides, a serializer built using CML mux-latch suffers from delay difference between the clock and data path [11]. Further, process, voltage and temperature (PVT) causes uncertainty in performances and varies the delay difference to introduce jitter in output eye. Inserting clock buffers in the clock path addresses the issue, but additional problem in terms of timing margin and layout area crop up. It is also observed that under identical biasing condition a mux-latch designed for a specific application generates time intervals

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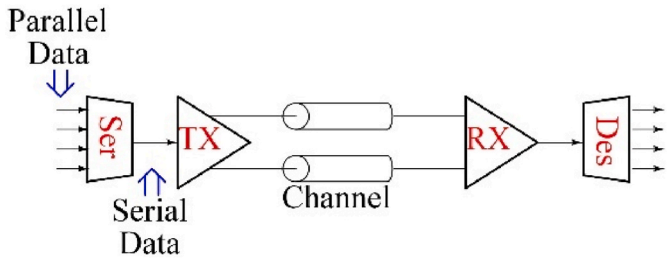


Fig. 1. Block diagram of a serial link transceiver with SerDes.

with different offset. Besides, in comparison to the externally applied Vdd the voltage V_P near the die due to power delivery network (PDN) is completely different and fluctuates with time due to Ldi/dt noise. This makes delay (t_d) estimation difficult for high-speed mux-latch. It is expected for a mux-latch to generate a constant t_d for a given process and Vdd. Nonetheless the V_P fluctuation makes the pulse edges to shift, thereby, results in t_d quite different than the V_P with no noise.

This made us to design a mux-latch at 90-nm CMOS, 1.1 V Vdd and switching at 16 GHz. If the operating frequency is increased beyond 16 GHz at 1.1 V and 27^{O}C, outputs deteriorate to drive other stages of the serializer. Accordingly, the present circuit is built using a combination of PMOS, NMOS gates while coupled to a power delivery network (PDN) to operate at 16 GHz. Being different from the CML or improved CML, performances are obtained for application which causes clock to be switched at 6.25 GHz. Subsequently, average power (P_{avg}), t_d, power delay product (PDP) and figure of merit (FoM) are obtained under PVT. Since mux-latch is often designed with other circuits sharing a common V_P, evaluating t_d of an oscillating system because of power supply droop due to PDN is essential. All the circuits do not operate at the same time and a significant amount of current is pumped in as some of them is turned on from idle state. The Ldi/dt noise so generated causes V_P to oscillate. Eventually, t_d and the jitter due to power supply noise (PSN) are estimated due to fluctuations in V_P. Based on the above discussions following sections are defined and will be discussed in the proposed paper. Section 2 describes the review of the mux-latch in the said technology as available in literature. It also highlights the issues of the conventional design in the said process and Vdd. Section 3 presents a new design coupled to a PDN and an analytical model to understand P_{avg}-t_d trade-off. Section 4 shows the post layout simulation results in a 90-nm CMOS, Vdd of 1.1 V and t_d variation with AC oscillating noise. To indicate mux-latch robustness, section 5 presents a 4:1 serializer in 90-nm CMOS and 1.1 V Vdd. Section 6 presents the performance comparison with other works and the conclusion in section 7 summarizes.

2. Literature

Alioto and Palumbo presented a CML mux built using BJT, operating within 6–20 GHz and a delay model to show dependencies with process parameters, external load and trade-off between system delay and power dissipation [12]. D. Kehrer, H. -D. Wohlmuth and Chen *et. al.* worked on transformer based 2:1 mux, where CML logic was split into two individual circuits to be inductively coupled and controlled [13,14]. The use of inductor increases layout area, average power and offers low voltage headroom. Raghavan *et. al.* suggested a modified mux circuit, where inductor was placed in series with load resistor and clock signals were stacked above the input transistors [15]. But it suffers from typical inductive circuit issues along with high clock to output delay due to clock loading effect. Gupta *et. al.* proposed CML based triple tail 2:1 mux and presented an analytical model to express system delay as the function of bias current and voltage swing [16]. The driver transistors create loading effect due to large device dimension, which increases delay and logic failure is very common when operating temperature varies. Venna presented a mux circuit with reset switch to eliminate residue charge in internal nodes [17]. The use of distinct transistors increases output voltage swing and operating frequency at the cost of high-power dissipation. Jang *et. al.* presented optimization technique to analyse and address power-performance trade-off in CML mux and latch [18]. Authors identified optimum input data rate, clock edge rate and inter-state voltage swing for minimal device sizing to obtain best fitting result at different technology nodes. Chattopadhyay *et. al.* proposed a low power source-series-terminated (SST) driver using a set of parallel logic gates, 2:1 static data mux and a series resistor [19]. The use of additional logic gates to retime input data increases the response time and area. He *et. al.* presented high speed 2:1 mux for Non-return to Zero (NRZ) transmitter operating at 40 Gb/s [20]. The presence of single–to-differential block before mux adds extra delay in output, which lead to frequent data bit loss and the inductor in series increases layout area. Neyestanak *et. al.* proposed the first CML mux-latch, but the concern is about large transistor stack [4]. The presence of cross coupled capacitor for preventing kick-back from latch increases the delay. Tsai *et. al.* presented another CML mux-latch to address the problems of existing design [21]. The time for a signal to transit from low to high or vice versa is one fourth of clock period, which is very less and allows intermediate states in output. Lovitt presented a 2:1 mux-latch with double cross-coupled logic and discretely arranged select lines for two inputs [22]. Circuit was designed for rail-to-rail swing at reasonably lower Vdd, but the double cross-couple adds extra parasitic to increase the response time and power dissipation. Suhani *et. al.* presented medium to high frequency CML based mux-dual latch to mitigate clock dependent latencies of the output [23]. However, there is always a direct path between Vdd and ground in one of the differential paths, which prevents the corresponding output from staying logic low.

Based on the above discussion, a new low power, PVT variation tolerant and low jitter mux-latch is proposed for serializer interface. The proposed design allows multiplexing and latch operation at the same time and does not require enable inputs to control latch operation. The elimination of additional gates to generate enable inputs reduces the gate count and provides higher output voltage headroom with low layout area. Mux-latch is often designed with other blocks in a serializer and none of the conventional designs have shown the effect of power supply noise on performance. The effective supply voltage V_P close to the circuit droops and oscillates with time when CPU core draws abrupt current. The Ldi/dt noise so generated introduces jitter and shifts the output voltage swing. It is imperative to understand the performance under AC noise and to observe the corresponding jitter.

3. A typical PDN and the proposed mux-latch coupled to PDN

The PDN along with the CPU core current I(t) is shown in Fig. 2a. Inductance L_{mb}, capacitance C_{mb} and resistance R_{mb} represent package pin and socket to connect PCB to constant Vdd. Apart from that they form path to Vdd whereas, resistance R_{skt} and inductance L_{skt} are a part of it. Inductance L_{pkg} denotes package inductance from C4 bump of silicon to package decoupling capacitance C_{pkg}. However, R_{pkg} implies effective resistance of decoupling capacitance and package traces. Beside, R_{via} and L_{via} represent via resistance and inductance, respectively, while R_{die} and C_{die} denote die resistance and de-coupling capacitance, respectively. In addition to so, I(t) serve as the current drawn by other blocks coming out from idle state or may be from sleep mode. It is interesting to mention that C_{die} maintains V_P close to Vdd and R_{die} regulates the oscillation amplitude. However, V_P droops with various PDN frequencies as I(t), the core current, is drawn suddenly, which severely affects t_d. The PDN in Fig. 2a imitates a regular CPU, where the maximum I(t) is about 10–30 A. Typically, it take 4–5 clock cycles to generate the said I(t). This work attempts to understand the working and performances of mux-latch coupled to PDN under PVT and during the period when V_P is droping and rising at various times.

Multiplexer (mux) latch is a circuit that admit both multiplexing and data retention depending on the state of enable input. Typically, mux is a

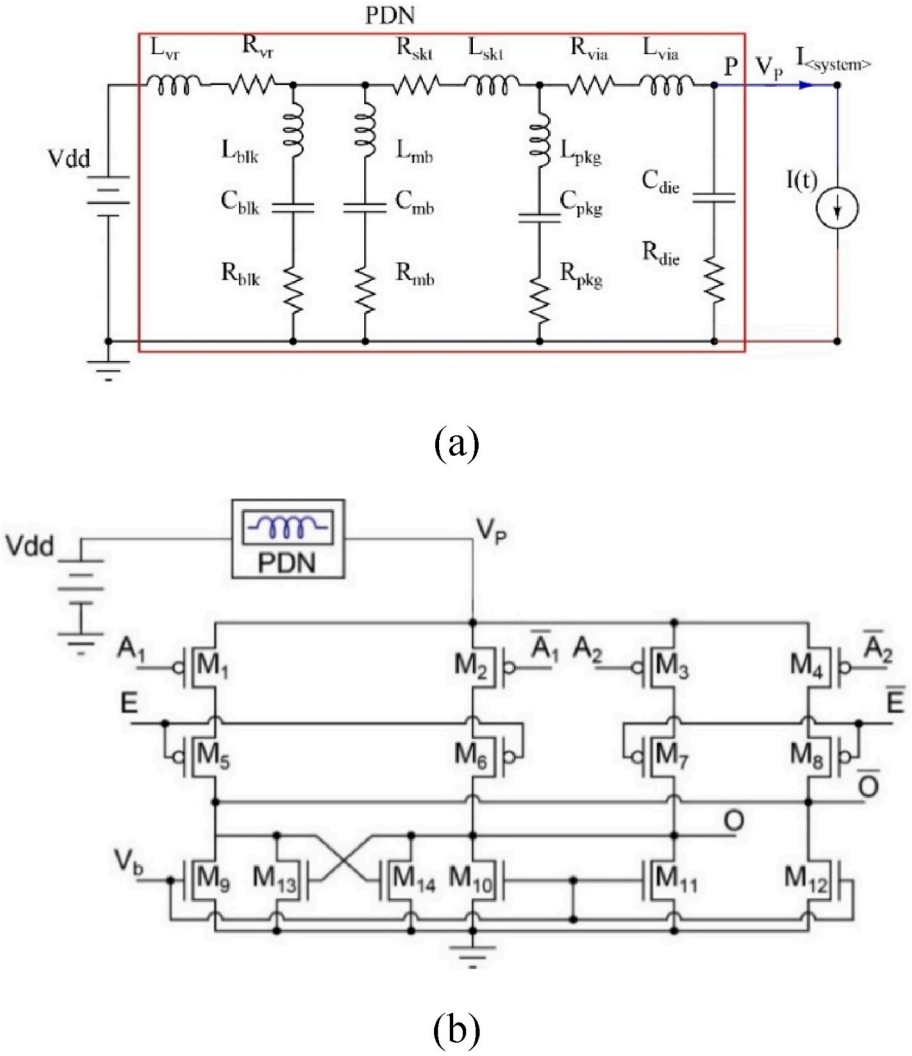


Fig. 2. a) Typical power delivery network (PDN) and b) the proposed 2:1 mux-latch coupled to PDN.

combinational circuit where enable line(s) determine an input among a set to be traversed to an output. Whereas, latch is a sequential block, where data sampling happens during half clock cycle and holds the state for the other half. Serializer requires mux to traverse data and latch to retain its state before being applied to next stage as shown in Fig. 1. Following this, a serialized output is obtained and fed into a driver (TX) as shown in the figure. In conventional serializer mux and latch operate independently to transmit data and retain the desired logic level. This increases circuit layout area, power and delay. Mux-latch avoids the use of multiple blocks of mux, latch, thereby results in a design with better outcome.

The schematic of the proposed mux-latch is shown in Fig. 2b. In the figure, an identical pair of PMOS M_1-M_4, M_5-M_8 and NMOS M_9-M_{12} constitute the mux while the latch is designed using NMOS M_{13}-M_{14} to retain the state of data irrespective of the enable input E. Normally, E allows either M_5-M_6 or M_7-M_8 to be turned on at a time while M_9-M_{10} and M_{11}-M_{12} are always on due to constant bias voltage V_b. Depending on the state of the inputs A_1 or A_2, outputs are available at O and $\overline{O}$. The outputs so obtained are retained indefinitely using the cross-coupled M_{13}-M_{14}. This is completely different from the conventional designs, where control input is required to enable latch to hold the state of the outputs.

A logic low at E turns on M_5-M_6 and allows differential data A_1 and $\overline{A}_1$ at the gate of M_1-M_2 to be available at the output. During this period, differential data A_2 and $\overline{A}_2$ at the gate of M_3-M_4 are not available because M_7-M_8 are off. Accordingly, A_1 = logic high turns off and on the corresponding gates and discharges $\overline{O}$ to logic low through M_9 and M_{12}. Whereas O charges to the effective supply voltage V_P through M_2 and M_6. Normally, a logic high at O turns on M_{13} and allows $\overline{O}$ to shift closer to logic low but M_{14} remains off as $\overline{O}$ is at logic low. Similarly, A_1 = logic low allows $\overline{O}$ to be charged to V_P through M_1 and M_5. However, O discharges to logic low through M_{10} and M_{11}. The state change is again retained using the cross-coupled M_{13}-M_{14}. An identical operation is also obtained when E switches to logic high. During this period, depending on the state of A_2 at the gate of M_3-M_4, M_7-M_8 determines the state of O and $\overline{O}$. It is evident that Fig. 2b is working as a mux, but the cross-coupled NMOS is working independently to hold the state of O and $\overline{O}$ to maintain the desired logic level. Besides, the cross-coupled NMOS mitigates the glitches in O and $\overline{O}$ due to rapidly slewing clock signal.

3.1. *Mathematical model to understand t_d dependency and P_{avg}-t_d trade-off*

The model serves as a foundation to derive delay between the control input E and output O during mux-latch operation i.e., E and $\overline{E}$ are low and high, respectively. When $\overline{E}$ remains high, M_7-M_8 are off and A_2 does not affect the outputs. Further, in a mux-latch only one direct path is available between effective power supply voltage V_P and output at a time while the complementary output discharges to ground. Thus, when

A_1 is considered to be low, $\overline{O}$ charges to logic high through M_1-M_5, while O discharges to ground through M_{10}-M_{11} and M_{14}. Though E enables M_6, but a logic low at A_1 turns off M_2 and there is no current path from V_P to M_6. Therefore, the capacitive effect of M_6 is considered only to derive the small signal model of the mux-latch while the on-resistance and path current are neglected as these have no significant effect on the overall circuit. Besides, O being logic low also turns off M_{13} and the capacitive effect is only considered in the small signal analysis.

The mux-latch with the corresponding parasitic capacitors, which significantly affect the individual gate operation is shown in Fig. 3a. The gate drain capacitance $C_{gd,}$ drain body capacitance C_{db} and source body capacitance C_{sb} are the parasitic capacitances across individual gate. The small signal model of Fig. 3a is shown in Fig. 3b, where g_m, g_{mb} are the *trans*-conductance, back-gate *trans*-conductance, respectively, and r_O is the output resistance due to channel length modulation. In addition to so, V_{in} denotes the voltage level at E and $\overline{E}$. The linearized small signal equivalent circuit after rearrangement of elements results in a simple model suitable for delay estimation as shown in Fig. 3c. Here, C_A, $C_{B,}$ $C_{C,}$ C_D and R_A, R_B are the equivalent capacitances and resistances, respectively, obtained in the process of circuit simplification and expressed as follows,

$$C_A = C_{gd1} + C_{bd1} + C_{bs5} \tag{1}$$

$$C_B = C_{db5} + C_{bd8} + C_{dg8} + C_{gd9} + C_{db9} + C_{db12} + C_{gd12} + C_{db13} \tag{2}$$

$$C_C = C_{gd13} + C_{gd14} \tag{3}$$

$$C_D = C_{db6} + C_{dg6} + C_{dg7} + C_{db7} + C_{db10} + C_{gd10} + C_{gd11} + C_{db11} + C_{db14} \tag{4}$$

$$R_A = \frac{r_{O9} \times r_{O12}}{r_{O9} + r_{O12}} \tag{5}$$

$$R_B = \frac{r_{O10} \times r_{O11} \times r_{O14}}{r_{O10}r_{O11} + r_{O11}r_{O14} + r_{O10}r_{O14}} \tag{6}$$

The process of delay estimation starts with the linearization of the proposed mux-latch and by replacing the gates by the small-signal model of Fig. 3a, where all the parasitic components are not considered. Only those which have significant effect on delay are the part of model. The equivalent linear circuit of a gate can be further simplified by replacing all the parallel capacitors and resistors with single equivalent capacitor and resistor, respectively. Now, single pole open circuit time constant τ is determined for all the capacitors. In open circuit time constant, one capacitor is considered at a time and remaining all the others are open circuited. Then the capacitor is replaced by a voltage source V_X from which a current I_X flows. The ratio of V_X and I_X determines the net resistance in the loop. Therefore, the product of the resistance and capacitance gives the open circuit time constant due to a specific capacitor. Lastly, the superposition of open circuit time constant gives the net propagation delay t_{PD} of the proposed mux-latch.

The open circuit time constant $\tau_{C_{gd5}}$ due to C_{gd5} can be derived as follows. Let,

$$\frac{V_X}{I_X} = r_X \tag{7}$$

where V_X and I_X are defined above. Applying KVL,

$$V_X - I_{rO5}r_{O5} - I_X r_{O1} = 0 \tag{8}$$

where I_{rO5} is the current across r_{O5}. Applying KCL at node A,

$$I_{rO5} = I_X - g_{m5}V_{gs5} - g_{mb5}V_{bs5} \tag{9}$$

Substituting equation (9) into (8) gives,

$$V_X = \left(I_X - g_{m5}V_{gs5} - g_{mb5}V_{bs5}\right)r_{O5} + I_X r_{O1} \tag{10}$$

where $V_{bs5} = -V_{s5}$, $V_b = 0$ and $V_{gs5} = V_{bs5} = -V_{s5}$. Using Fig. 3c, following substitution and simplification,

$$\frac{V_X}{I_X} = r_X = \{(1 + g_{m5}r_{O5} + g_{mb5}r_{O5})r_{O5} + r_{O1}\} \tag{11}$$

Also,

$$r_X \parallel R_A = R_1 \tag{12}$$

Therefore, the time constant due to C_{gd5} is written as,

$$\tau_{C_{gd5}} = R_1 C_{gd5} \tag{13}$$

The open circuit time constant $\tau_{C_{gs5}}$ due to C_{gs5} can be derived as follows,

Applying KCL at node A,

$$I_X + g_{m5}V_{gs5} + g_{mb5}V_{sb5} - \frac{(V_X - I_X R_A)}{r_{O5}} = 0 \tag{14}$$

Substituting $V_g = 0$, $V_{gs5} = -V_X$ and after simplification,

$$\frac{V_X}{I_X} = r_X = \frac{\left(1 + \frac{R_A}{r_{O5}}\right)}{\left(g_{m5} + g_{mb5} + \frac{1}{r_{O5}}\right)} \tag{15}$$

Also,

$$r_X \parallel r_{O1} = R_2 \tag{16}$$

Therefore, the time constant due to C_{gs5} is given by,

$$\tau_{C_{gs5}} = R_2 C_{gs5} \tag{17}$$

The open circuit time constant τ_{C_A} due to C_A can be derived following the steps to determine $\tau_{C_{gd5}}$,

$$\frac{V_X}{I_X} = r_X = \frac{\left(1 + \frac{R_A}{r_{O5}}\right)}{\left(g_{m5} + g_{mb5} + \frac{1}{r_{O5}}\right)} \tag{18}$$

Also,

$$r_X \parallel r_{O1} = R_2 \tag{19}$$

Therefore, the time constant due to C_A is written as

$$\tau_{C_A} = R_2 C_A \tag{20}$$

The open circuit time constant τ_{C_B} due to C_B can be obtained as follows,

Applying KCL at node A,

$$I_X - g_{m5}V_{gs5} - g_{mb5}V_{sb5} - \frac{V_X - (-V_{gs5})}{r_{O5}} = 0 \tag{21}$$

Using Fig. 3c, substituting $V_{gs5} = V_{sb5}$, $V_{gs5} = -I_X r_{O1}$ and after simplification (21) reduces into,

$$\frac{V_X}{I_X} = r_X = r_{O5}\left\{1 + r_{O1}\left(g_{m5} + g_{mb5} + \frac{1}{r_{O5}}\right)\right\} \tag{22}$$

Also,

$$r_X \parallel R_A = R_3 \tag{23}$$

Therefore, the time constant due to C_B is written as,

$$\tau_{C_B} = R_3 C_B \tag{24}$$

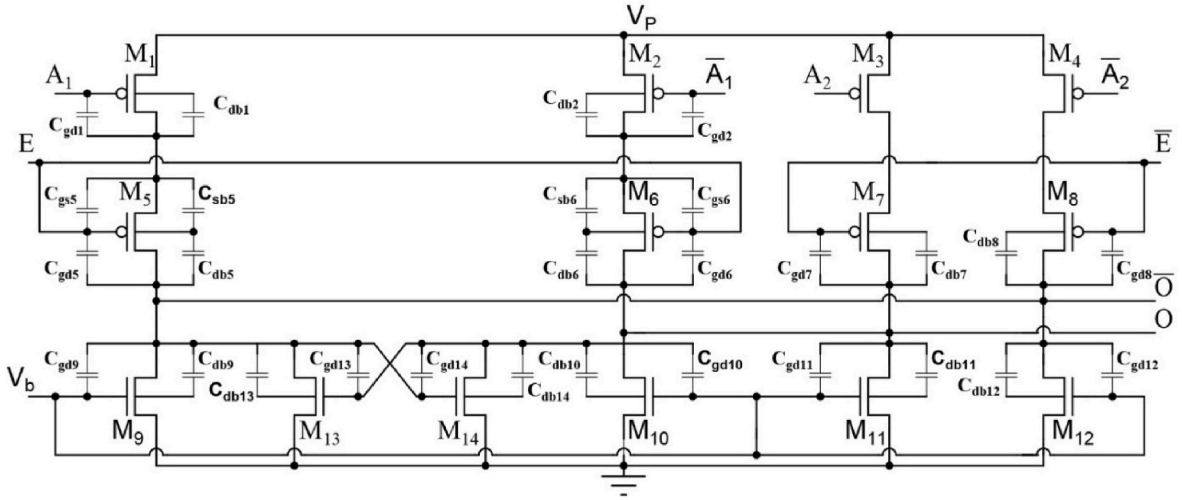
The open circuit time constant τ_{C_C} due to C_C can be obtained as given,

Applying KCL at node A,

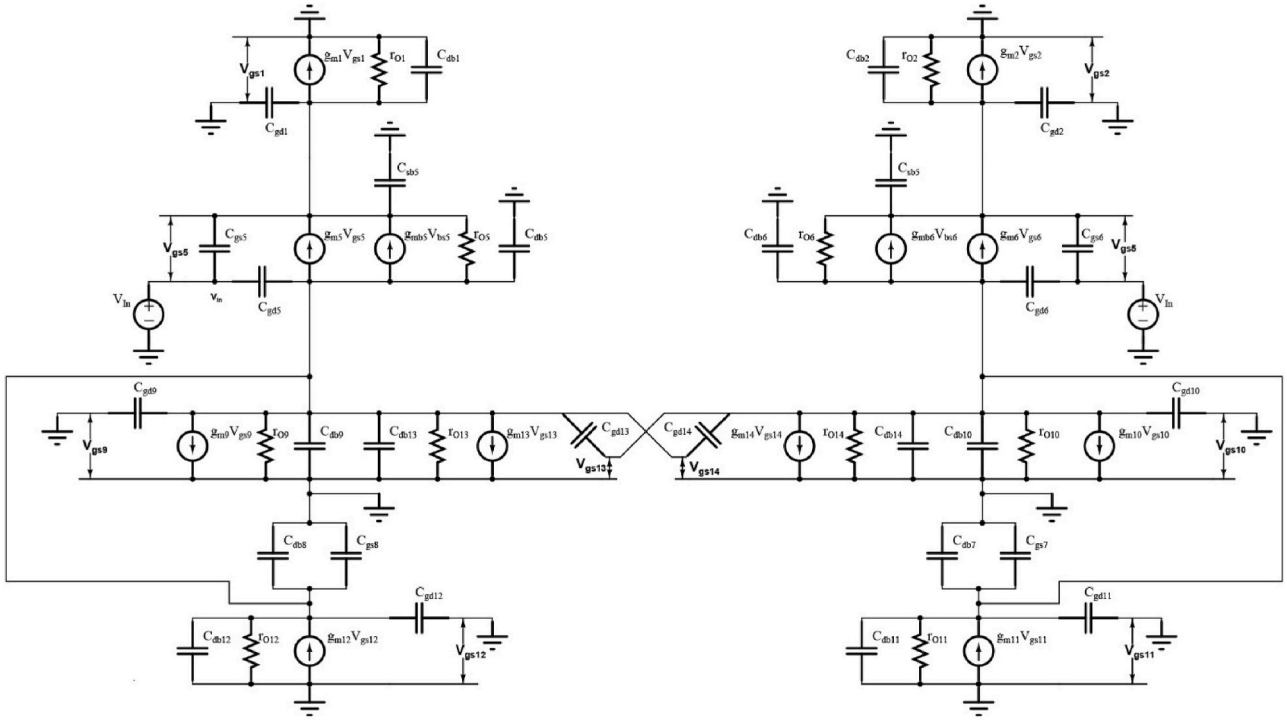
$$-\frac{V_1}{R_A} - \frac{(V_1 - V_{s5})}{r_{O5}} - g_{m5}V_{gs5} - g_{mb5}V_{sb5} + I_X = 0 \tag{25}$$

Substituting $V_{gs5} = V_{sb5}$ simplifies (25) into,

$$V_1\left(\frac{1}{R_A} + \frac{1}{r_{O5}}\right) = \frac{V_{s5}}{r_{O5}} - (g_{m5} + g_{mb5})V_{gs5} + I_X \tag{26}$$



(a)



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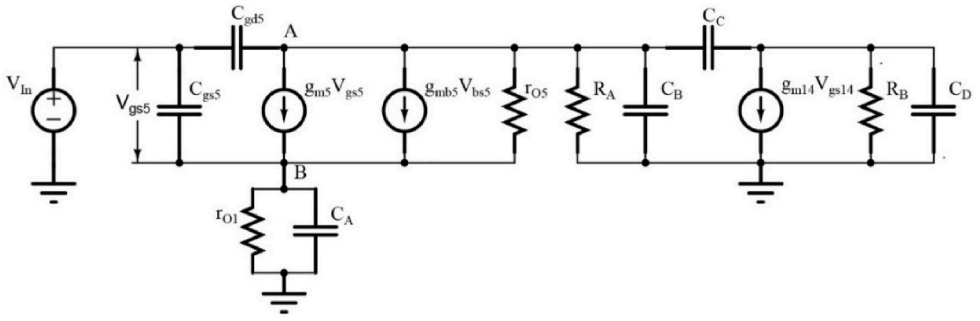

(c)

Fig. 3. Proposed mux-latch a) with parasitic capacitors, b) corresponding small signal equivalent circuit and c) simplified small signal equivalent circuit to estimate t_d.

Applying KVL,

$$V_X = V_1 + \left(g_{m14} V_{gs14}\right) R_B \tag{27}$$

Substituting $V_{gs14} = V_1$ in (27) and replacing V_1 in (26) gives,

$$\left(\frac{V_X}{1 + g_{m14} R_B}\right)\left(\frac{1}{R_A} + \frac{1}{r_{O5}}\right) = V_{s5}\left(\frac{1}{r_{O5}} + g_{m5} + g_{mb5}\right) + I_X \tag{28}$$

Applying KCL at node B,

$$\frac{r_{O1}}{r_{O5}} V_1 = V_{s5}\left\{1 + (g_{m5} + g_{mb5}) r_{O1} + \frac{r_{O1}}{r_{O5}}\right\} \tag{29}$$

Substituting V_1 in (29) and then V_{s5} in (28) gives,

$$\frac{V_X}{I_X} = r_X = \frac{1 + g_{m14} R_B}{\left(\frac{1}{R_A} + \frac{1}{r_{O5}}\right) - \frac{\frac{r_{O1}}{r_{O5}}}{\left\{1 + (g_{m5} + g_{mb5}) r_{O1} + \frac{r_{O1}}{r_{O5}}\right\}}\left(\frac{1}{r_{O5}} + g_{m5} + g_{mb5}\right)} \tag{30}$$

Therefore, the time constant due to C_C is written as,

$$\tau_{C_C} = r_X C_C \tag{31}$$

The open circuit time constant due to C_D is written as,

$$\tau_{C_D} = R_B C_D \tag{32}$$

The propagation delay t_{PD} of the mux-latch is the sum of the individual open circuit time constants,

$$t_{PD} = \tau_{C_{gd5}} + \tau_{C_{gs5}} + \tau_{C_A} + \tau_{C_B} + \tau_{C_C} + \tau_{C_D} \tag{33}$$

It is also worth to mention that the open circuit single pole method of delay estimation is linearly related with the time constant of the circuit.

4. Simulation results and analysis

The parasitic components of the PDN of Fig. 2a are tabulated in Table 1. Using the analytical model, the gate sizes in Table 2 are chosen to understand the working of Fig. 2b with fast slewing control input *E*. Typically, Table 2 presents the values to obtain a comparable t_d without degrading P_{avg}. The layout of the gates of Fig. 2b is shown in Fig. 4a. The estimated area is about 14.7 × 10.5 μm^2 without the bond pad and die de-coupling capacitor. Simulated in a 90-nm CMOS and 1.1 V Vdd, the post-layout transient corresponding to inputs A_1, A_2 switching at 3.125 GHz and $E = 6.25$ GHz is plotted in Fig. 4e. The rise, fall times are about 20 ps and 10 ps, respectively. It is observed that as *E* is at logic low, A_1 is forwarded to the output *O* and retained using the cross-coupled gates. But, as *E* switches to logic high, A_2 is forwarded to the *O* and retained until *E* changes back. Therefore, for a typical (NN) process P_{avg}, t_d and power delay product (PDP) are noted to be 257.7 μW, 35 ps and 9 fJ, respectively. A figure of merit (FoM) is also defined using (34) to indicate mux-latch robustness [24]. It is imperative to reduce FoM for a given process, Vdd, junction temperature and the value is about 65 ns × fJ × μm^2.

$$FOM = EDP \times Area \times \frac{Voltage\ Swing}{Noise\ Margin} \tag{34}$$

Subsequently, Table 3 tabulates the outcome of the present mux-latch at no skew and 5% skew. The mean (μ) and standard deviation (σ) are also shown assuming a 5% fluctuation of the allowed value in Vdd. There are also jitter concerning rise, fall times of the signal appearing between 5%. At distinct corners (NN, SS, FF) the P_{avg} is found to be varying for a fixed Vdd, thus ranging between 313.7 μW for FF to 210.2 μW for SS. However, the difference in data for t_d, PDP and FOM at distinct corner is small. The t_d, PDP and FOM are highest for SS, where 3σ is about 2.7 ps, 0.6 fJ and 0.6 ns × fJ × μm^2, respectively. The histogram of P_{avg}, t_d and PDP are plotted for NN process while performing Monte Carlo study on the proposed mux-latch, Fig. 5. The metrics are same to that of the data from NN process.

Table 1
PDN parasitic values.

Inducatnces	L_{vr} 1 nH	L_{blk} 1 nH	L_{mb} 300 pH	L_{pin} 50 pH	L_{pkg} 30 pH	L_{via} 20 pH	– –
Resistances	R_{vr} 1 mΩ	R_{blk} 2 mΩ	R_{mb} 0.5 mΩ	R_{pin} 0.2 mΩ	R_{pkg} 1 mΩ	R_{via} 0.2 mΩ	R_{die} 1 mΩ
Capacitances	– –	C_{blk} 1.5 nF	C_{mb} 0.1 nF	– –	C_{pkg} 0.02 nF	– –	C_{die} 100 nF

Table 2
Gate sizes of the proposed 2:1 mux-latch.

M_{1-4}	M_{5-8}	M_{9-12}	M_{13-14}
2.1 μm/100 nm	1.8 μm/100 nm	0.35 μm/100 nm	0.55 μm/100 nm

The μ and σ of noise margin low (NM_L) and high (NM_H) at different corners (NN, SS, FF) and temperature are tabulated in Table 4. The noise margin values are observed to be independent of temperature. Accordingly, a mux-latch is designed to have no temperature dependency while μ of the corners is considered. Fig. 6a shows a monotonic drop in P_{avg} with junction temperature at different corner. A drop in P_{avg} by 47 μW, 33 μW and 64 μW, respectively, is evident as temperature changes by 117^OC. This refers to about 0.3 μW drop for 1^OC rise in temperature. However, t_d is noted to increase by 8 ps, 5ps and 14 ps, respectively, for a temperature change of 117^OC as shown in Fig. 6b. This corresponds to about 0.1 ps increase for 1^OC rise in temperature. In addition to so, PDP also increases with temperature change and conform to about 0.01 fJ rise for 1^OC increase in temperature as shown in Fig. 6c. Besides, Fig. 6d shows that a 117^OC change in temperature at different corner allows FOM to vary between 8.85ns × fJ × μm^2 and 45 ns × fJ × μm^2 for FF and SS, respectively.

A conventional increase in P_{avg} with Vdd at distinct corner (NN, SS, FF) is observed as shown in Fig. 7a. Therefore, Vdd change of 0.75–1.1 V allows P_{avg} to vary between 75 μW for SS and 313 μW for FF. Accordingly, 1 mV drop in Vdd allows P_{avg} to reduce by about 0.5 μW. Fig. 7b shows that at different corner t_d varies by 7 ps, 12ps and 3 ps, respectively, as Vdd is switched from 0.75 to 1.1 V. This confirms to a rise of about 0.02ps for 1 mV drop in Vdd. Besides, PDP is also noted to increase as Vdd changes from 0.75 V to 1.1 V and confirms to a drop of about 0.01 fJ for 1 mV drop in Vdd as shown in Fig. 7c. Lastly, Fig. 7d shows FOM to change by 26 ns × fJ × μm^2, 51.5 ns × fJ × μm^2 and 20ns × fJ × μm^2, respectively at different corner as Vdd varies between 0.75 V and 1.1 V.

Fig. 8a presents the output eye diagram of the proposed mux-latch. The benefit of the eye diagram is established in terms of parameters as tabulated in Table 5. Eye height and width are the most important parameter to describe how sensitive is the margin for the output voltage and timing jitter. The eye opening is about 910.9 mV and jitter is within 0.003–0.05 ps. Normally, jitter is very small when one operates at 5 GHz. Even the rise and fall times are bigger than the jitter, which simply rattles the rise and fall time. The separation of the mid points of two consecutive eyes as shown in Fig. 8a can be used to determine the operating frequency of the mux-latch. This corresponds to 6.25 GHz. The σ of the eye height is about 20 ps and is quite low given the eye height 789.7 mV. The clear separation between logic 0 and logic 1 is shown in Fig. 8b to indicate a very low BER ($<10^{-13}$) because the distribution does not overlap. Further, the clock period is noted to be (2 × 70.3) ps and this confirms to 7.11 GHz. However, sampling data with BER close to 10^{-13} requires both random and deterministic jitters. Therefore, (35) is used to calculate the actual jitter T. The post-layout white noise also referred to as the Johnson noise is plotted in Fig. 8c and d for different temperature and Vdd. It is important to mention that at both constant Vdd and temperature, white noise reduces at high frequency.

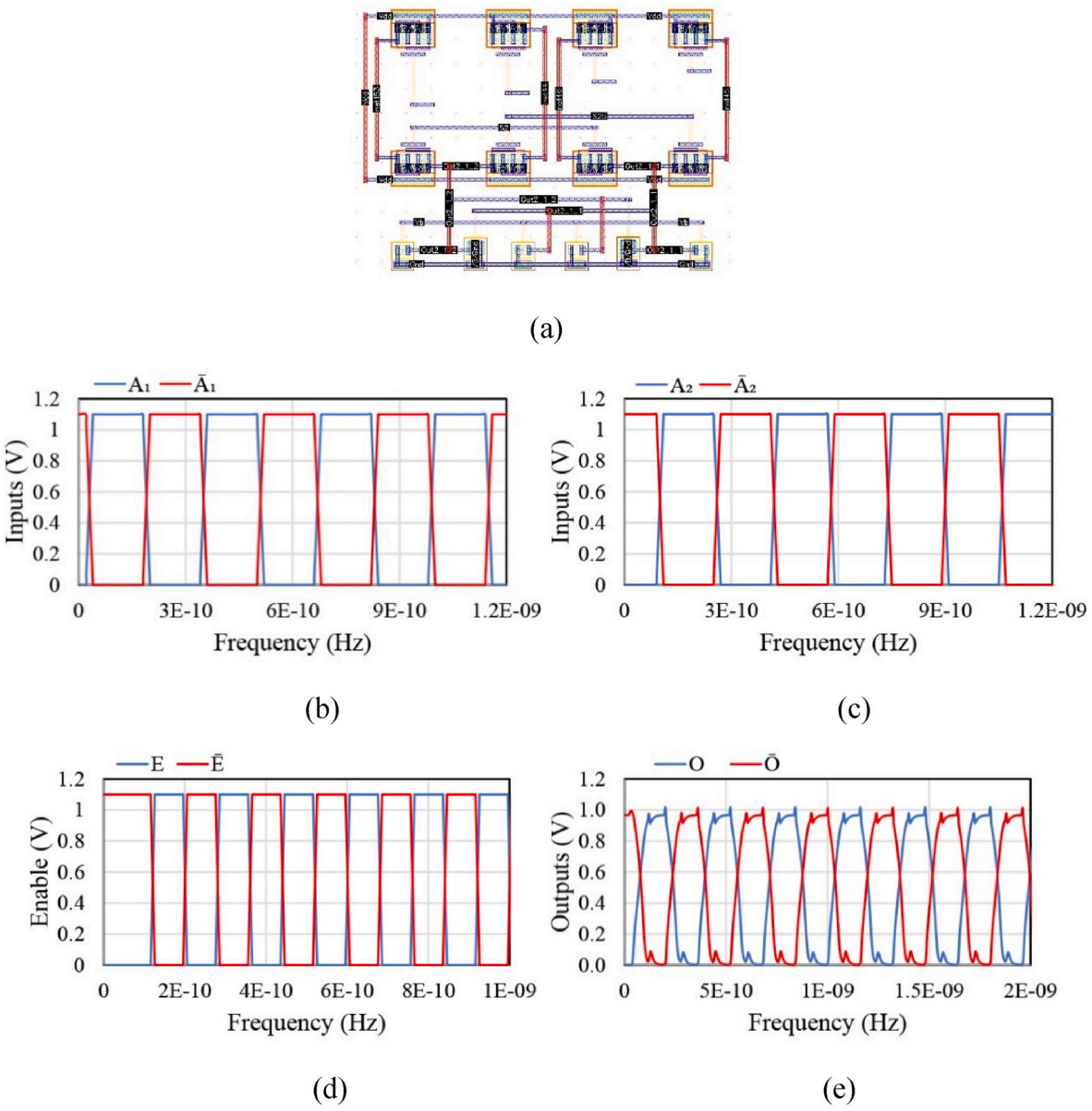

Fig. 4. a) Layout of the proposed mux-latch and b-e) timing diagram.

Table 3
Performances in post-layout.

Process & corner		P_{avg} (μW)		t_d (ps)		PDP (fJ)		FOM (ns × fJ × μm^2)	
No skew	NN	257.7		35		9		65	
	SS	210.2		53		11		120.2	
	FF	313.7		26		8.2		44.3	
		μ	σ	μ	σ	μ	σ	μ	σ
5% skew	NN	257.8	9.2	35.2	0.5	9.1	0.2	65	0.2
	SS	210.3	8.0	53.0	0.9	11.0	0.2	120.2	0.2
	FF	313.8	10.8	26.2	0.3	8.2	0.2	44.3	0.2

$$T = Determinictic\ jitter + 2n \times Random\ jitter \quad (35)$$

4.1. Delay (t_d) analysis with AC oscillating noise

The effective supply voltage V_P is observed, Fig. 9a, as the PDN draws an abrupt current I(t), 0–10 A, 20 A and 30 A in 10 ns. Subsequently, the output O variation is noted as shown in Fig. 9b, c, d and the corresponding t_d is evaluated due to I(t). To estimate t_d the output O is examined as V_P varies from 1.1 V to AC first droop and back to 1.1 V as shown in Fig. 9b, c, d. Accordingly, the t_d between the input A_1 or A_2 and O with V_P having no noise is denoted by ρ. Thereafter, the t_d as V_P reaches AC first droop is denoted by η. This corresponds to a V_P of 1.01 V, 0.912 V and 0.819 V, respectively, following I(t). The t_d due to AC first droop is different than the no noise and happens between 10 and 15 ns. A t_d same as no noise is obtained as V_P rises form AC first droop.

The t_d along with the AC first droop due to I(t) are tabulated in the third and first column of Table 6. Further, t_d is also estimated as Vdd in Fig. 2b is replaced with AC first droop and V_P having no fluctuations. Subsequently, the seventh column in Table 6 tabulates the t_d due to the DC voltages. These are same as the AC first droop due to I(t). It is worthy to state that the t_d due to DC are quite close to that obtained with AC noise. Eventually the t_d due to no noise, Vdd constant at 1.1 V, is found to be quite close to the t_d due to 0–10 A in 10 ns and the corresponding DC. However, difference in t_d arises beyond that. The filtering effect is responsible to this because the gate switching noise is small in

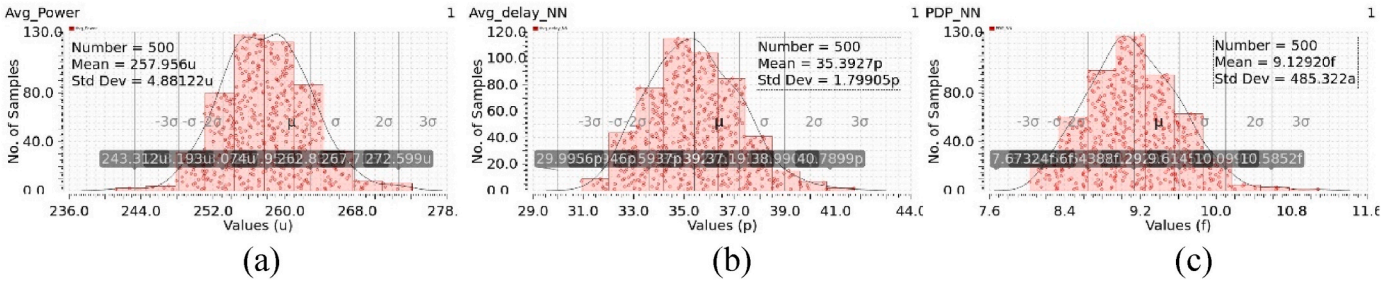

Fig. 5. Plot of Monte Carlo analysis a) P_{avg}, b) t_d and c) PDP with no skew in Table 3.

Table 4
Noise Margin variation with temperature in post-layout.

Temperature (°C)	NM_L (V)		NM_H (V)	
	μ	σ	μ	σ
−27	0.5	0.01	0.3	0.001
0	0.5	0.01	0.2	0.002
27	0.5	0.01	0.2	0.002
54	0.5	0.01	0.2	0.002
90	0.5	0.01	0.2	0.002

comparison to the voltage drop as the critical point is attained by the noise voltage. The standard deviation of the time period fluctuation is referred to as jitter. It is estimated by noting the fall time during the period noise shifts from the minimum to no voltage drop. The jitter due to AC noise and DC are tabulated in fourth and eighth column of Table 6. Fig. 10 shows that the jitter rises linearly with AC first droop, also referred to power supply noise.

5. 4:1 serializer using the proposed 2:1 mux-latch

Serializer is used to serialize a set of parallel data before being fed into a driver, Fig. 1. The process of serialization not only reduces the number of channels required for data transmission but also increases the data rate for both on chip and chip-to-chip communication. Conventional designs require 3 mux and 9 latch to design a 4:1 serializer. However, the design complexity reduces significantly with the use of mux-latch. Mux-latch makes on chip and chip-to-chip communication reliable and easier at the cost of reduced layout area and power. The block diagram of 4:1 serializer using the proposed 2:1 mux-latch, is shown in Fig. 11a. It is observed that two of the 2:1 mux-latches, A and B, are operating at a frequency of $f/4$ while the third one C at a frequency of $f/2$. In addition to that, parallel set of differential data are available at the inputs $I_1, \bar{I}_1$ and $I_2, \bar{I}_2$ of the A and B switching at $f/4$. The corresponding outputs O and $\overline{O}$ are then fed into the C switching at $f/2$ to obtain serialized outputs. Normally, the frequencies $f/2$ and $f/4$ are obtained from an external clock using two frequency dividers (FDs) as shown in the figure. The $f/4$ and $f/2$ are applied at the input E to enable the mux-latch A, B and C, respectively, to serialize the corresponding inputs.

Control input E enables the 2:1 mux-latch A and B following the arrival of $f/4$. However, the data at the I_1, $\bar{I}_1$ and I_2, $\bar{I}_2$ are traversed depending on the state of E. A logic low at E allows the I_1 of the A and B to be available at the O and $\overline{O}$ of the corresponding 2:1 mux-latch. Whereas E = logic high allows I_2 of the A and B to be available at the O and $\overline{O}$. Besides, the 2:1 mux-latch C is enabled on application of $f/2$ at E. But, the state of E determines the data transfer from the input to output. Accordingly, a logic high and low at E allows the I_1 and I_2, respectively, of the C to be available at the O and $\overline{O}$. Subsequently, the parallel data at the inputs are serialized.

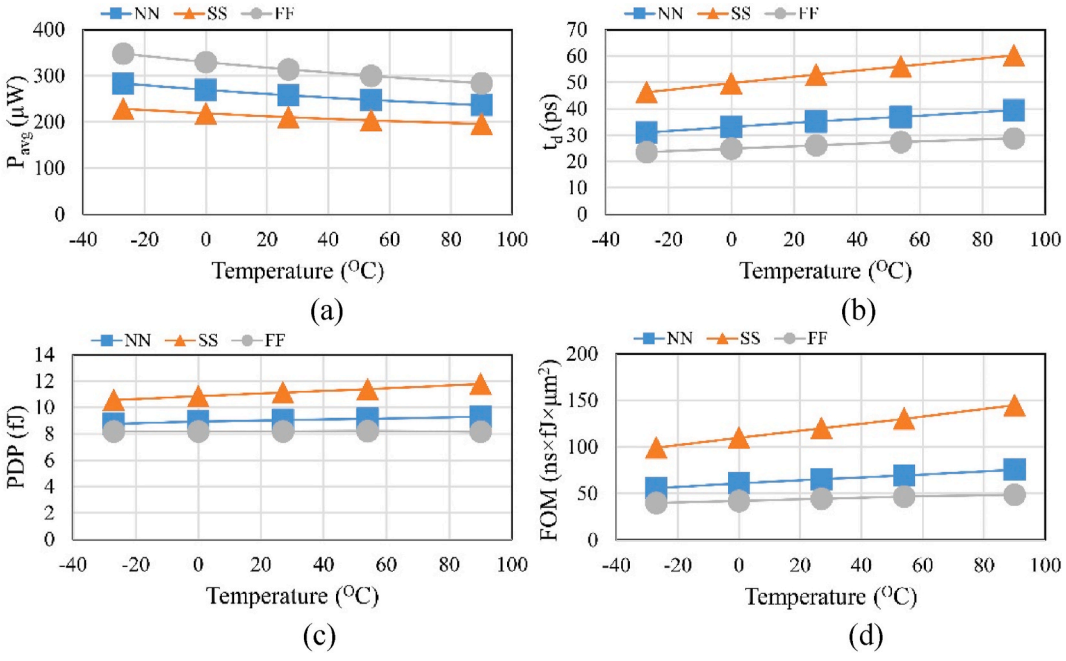

Fig. 6. Performance shift with temperature a) P_{avg}, b) t_d, c) PDP and d) FOM at 1.1 V Vdd.

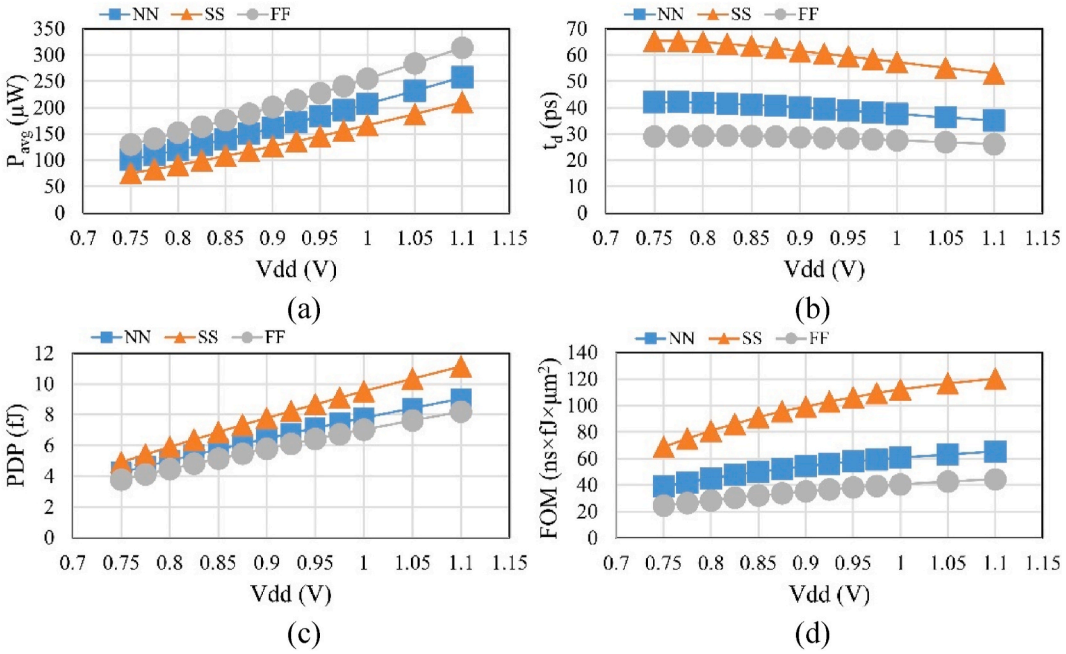

Fig. 7. Performance shift with Vdd a) P_{avg}, b) t_d, c) PDP and d) FOM at 27^{O}C.

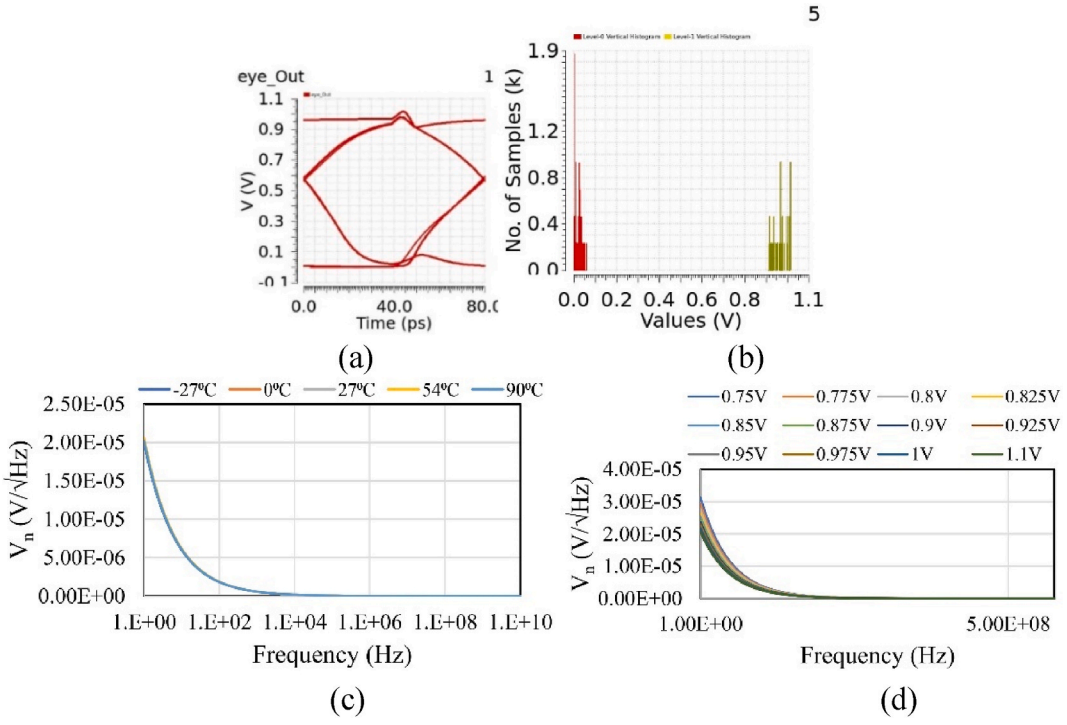

Fig. 8. a) Output eye @ 6.25 GHz, b) histogram, V_n variation at different c) temperature and d) Vdd.

5.1. Performances evaluation and analysis

The layout of the gates to design Fig. 11a is shown in Fig. 11b. The corresponding area without the bond pad and die decoupling capacitor is 54.5 × 49 µm^2. Besides, there are eight external inputs, one clock input and two outputs in Fig. 11b while sharing a single effective power supply V_P and ground. Simulated in a 90-nm CMOS and Vdd of 1.1 V, Fig. 12b, c, d illustrates the post-layout transient corresponding to an external clock f switching at 4 GHz. Fig. 12b shows the output of FD corresponding to $f/2$ switching at 2 GHz and Fig. 12c to that of the FD output switching at 1 GHz. Following the application of $f/4$ and $f/2$ as shown in Fig. 11a, the serialized output is shown in Fig. 12d. Subsequently, the P_{avg}, t_d and PDP of the 4:1 serializer are noted to be 6.2 mW, 54,0ps and 335.8 fJ, respectively. It is worthy to mention that the P_{avg} is due to both the 4:1 serializer and FD as shown in Fig. 11a. The histograms of P_{avg}, t_d and PDP of Fig. 11a are plotted in Fig. 13 for NN process. The P_{avg} and t_d are identical to the no skew data and PDP has shifted less than 1%. The performances variation with temperature at different corner (NN, SS, FF) are shown in Fig. 14. The P_{avg} varies between 3.8 µW for SS to 9.2 µW for FF. Increase in t_d as shown in Fig. 14b

Table 5
Output eye data in post-layout.

Parameters	Value
Threshold crossing Average (ps)	40.0
Threshold crossing stddev (ps)	35.2
Level 0 mean (mV)	36.6
Level 0 stddev (mV)	15.5
Level 1 mean (mV)	947.5
Level 1 stddev (mV)	25.0
Eye amplitude (mV)	910.9
Eye height (mV)	789.7
Eye Width (ps)	70.3
Eye S/N	22.5
Eye Rise Time (ps)	42.0
Eye Fall Time (ps)	49.0
Random Jitter (left) (ps)	0.047
Random Jitter (right) (ps)	0.003
Deterministic jitter (ps)	6.02

is mainly attributed to the P_{avg} increase. Normally, a change in temperature by 117^{O}C allows t_d to change by 28.3 ps, 45.7ps and 11.4 ps, respectively, at different corner. This confirms to a drop of about 0.2ps for1^{O}C drop in temperature. The PDP is noted to vary between 12.8 fJ for FF and 70.2 fJ for SS as the temperature switches from −27^{O}C to 90^{O}C.

Fig. 15a shows a conventional increase in P_{avg} with Vdd at NN, SS and FF. A Vdd change of 0.85–1.1 V allows P_{avg} to vary between 2.6 mW for SS and 7.8 mW for FF. This corresponds to a drop of 0.01 mW for 1 mV drop in Vdd. In addition to so, at different corner t_d varies by 2 ps, 20ps and 0.5 ps,

respectively, as Vdd is switched from 0.85 to 1.1 V, Fig. 15b. This confirms to a rise of about 0.01 ps for 1 mV drop in Vdd. Besides, PDP is also noted to increase as Vdd changes from 0.85 V to 1.1 V and confirms to a drop of about 0.3 fJ for 1 mV drop as shown in Fig. 15c. The out eye of the proposed 4:1 serializer is shown in Fig. 16a. Table 7 tabulates the goodness of the eye diagram, where the most important parameters are the eye height and width. These are used to describe the sensitivity of the output voltage margin and timing jitter. The eye opening is about 894.2 mV and jitter is within 0.31–2.3ps. The rise and fall times are larger than the jitter and jitter simply rattles the rise and fall time. The σ of the eye height is about 34 ps and is quite low for the given eye height of 692.2 mV. The clear margin for logic 0 and logic 1 is shown in Fig. 16b to indicate a very low BER ($<10^{-13}$) because the distribution does not overlap.

Table 6
t_d and jitter due to AC noise and DC.

ΔV_{min} (V)	Current ramps I(t)	t_d (ps)	Jitter (ns)	ΔV_{min} (V)	DC (V)	t_d (ps)	Jitter (ns)
0.281	1.1V_0-30 A	42.2	1.4	0	0.819	41.2	0.4
0.188	1.1V_0-20 A	40.5	1.1		0.912	39.8	0.2
0.09	1.1V_0-10 A	37.5	0.68		1.01	37.4	0.014
0	1.1V_0 A	35	0.7		–	–	–

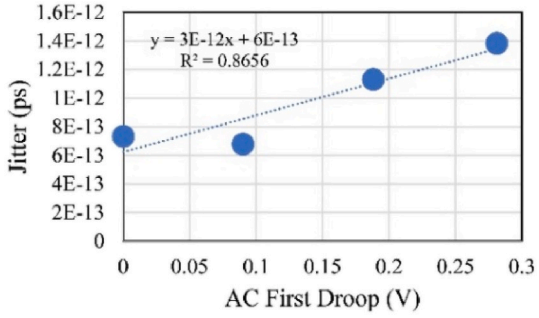

Fig. 10. Plot showing jitter as a function of AC first droop.

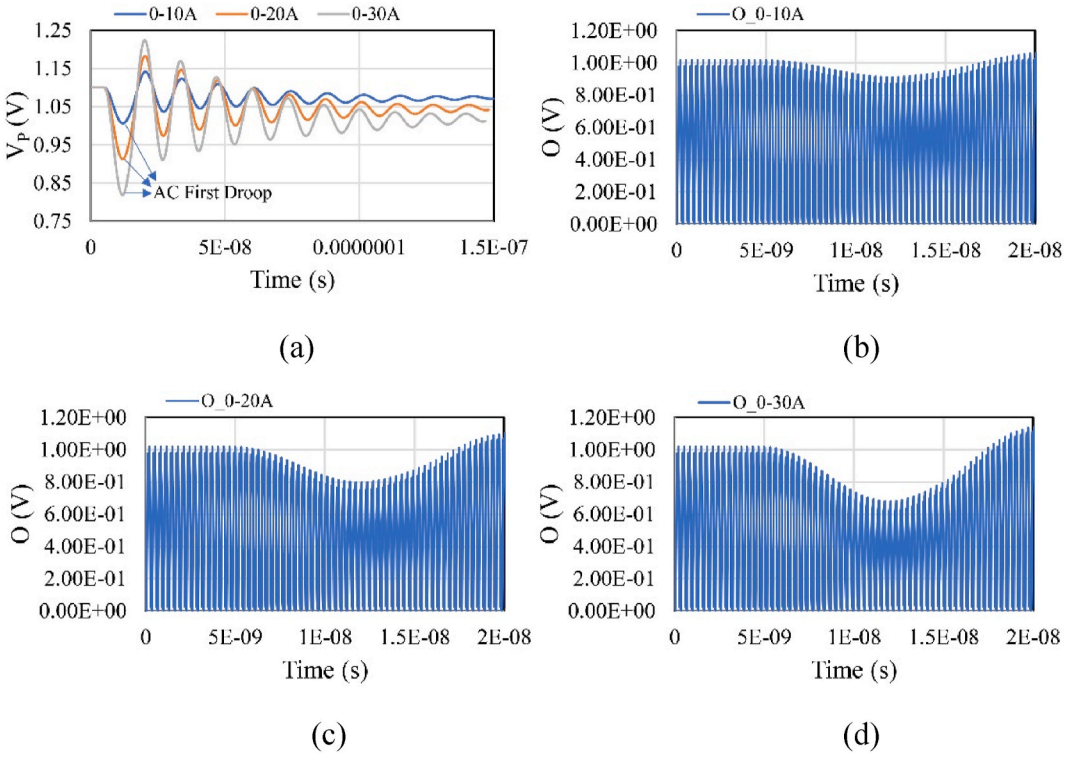

Fig. 9. Plot of a) V_P, output due to b) 0–10 A, c) 0–20 A and d) 0–30 A in 10 ns.

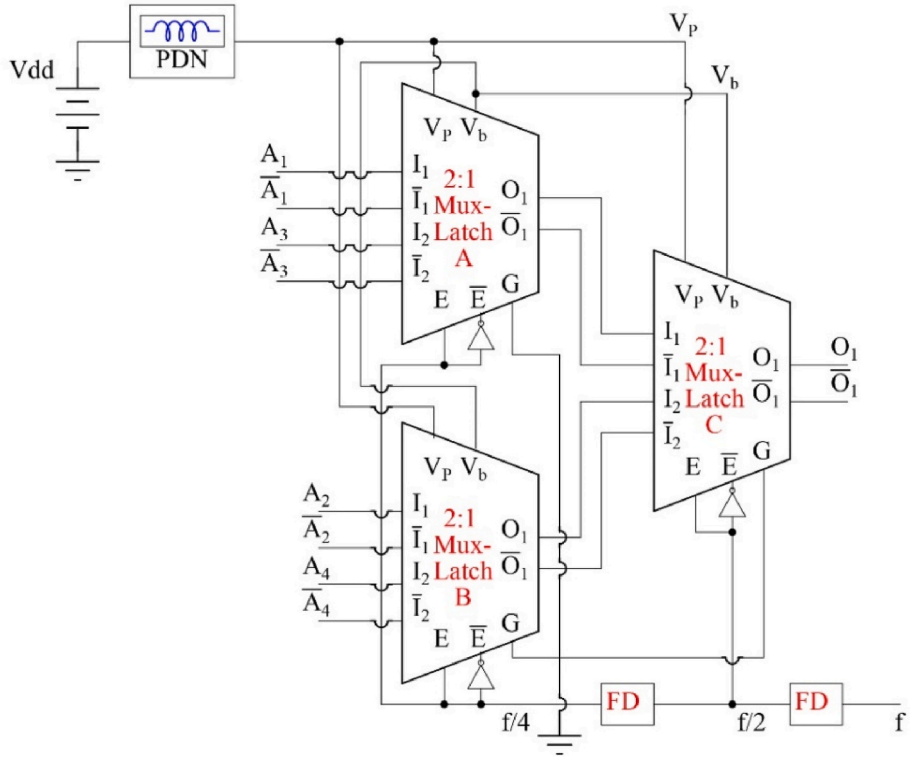

Fig. 11. a) Block diagram and b) layout of 4:1 serializer.

6. Performance comparison

The performance of the proposed 2:1 mux-latch and serializer along with conventional designs is tabulated in Table 8. To obtain a fair comparison, circuits in Refs. [4,21,23] are designed and simulated using the set-up used to analyse the proposed design. Following this, the process file and feature used are presented in the first and second row, while the third and fourth row shows the function and Vdd, respectively. It is interesting to mention that the proposed 2:1 mux-latch attains a voltage swing of 965 mV at 6.25 GHz. The corresponding value is 943 mV for the 4:1 serializer.

at 4 GHz. However, [4,21,23], obtained a voltage swing of 933 mV, 1000 mV and 915 mV, respectively, at the said process, Vdd and frequency. Even though [21] obtained the highest voltage swing at a given process and Vdd, the delay, average power, PDP and FOM are quite high. The same is also true for [4,23]. The elimination of additional gates to generate enable input simplifies the proposed design significantly. Eventually, this results in lowest average power and area among all the designs as shown in Table 8. Typically, the average power includes the CPU core switching current, 10A or more through PDN and the

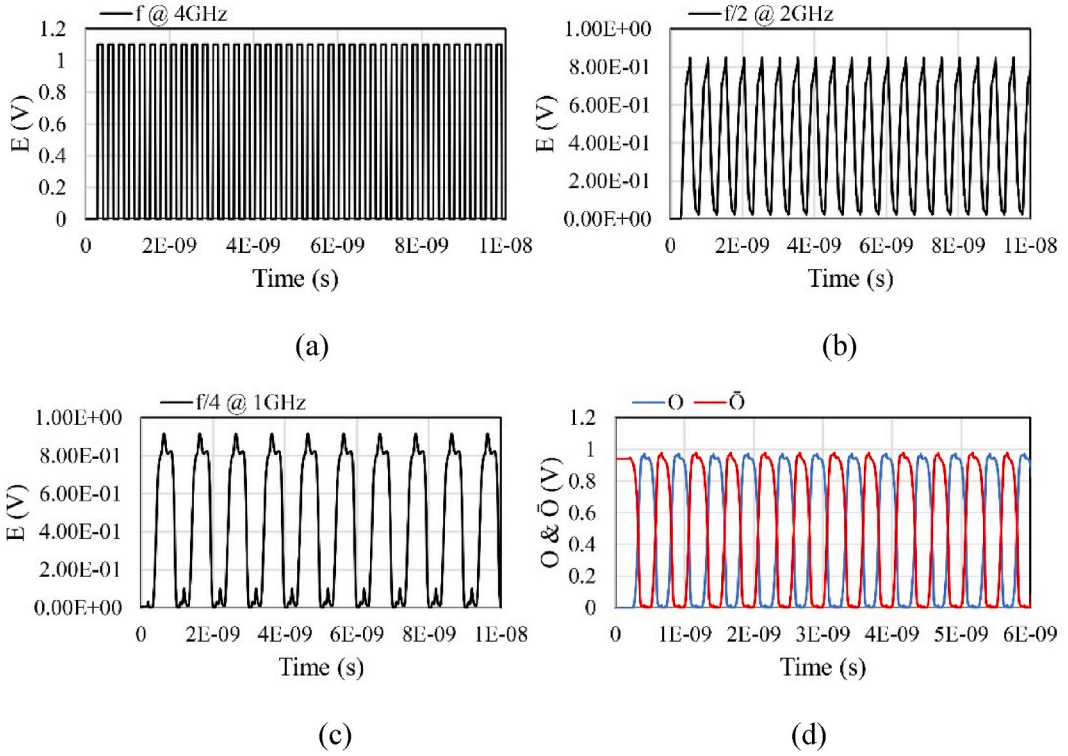

Fig. 12. Plot of enable *E* a) *f* @ 4 GHz, b) *f*/2 @ 2 GHz, c) *f*/4 @ 1 GHz and d) *O* of 4:1 serializer.

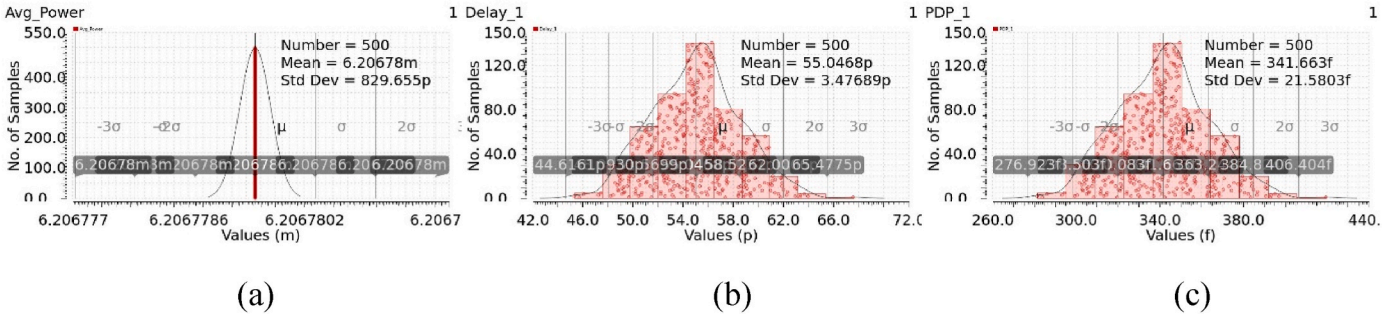

Fig. 13. Plot of Monte Carlo analysis of 4:1 serializer a) P_{avg}, b) t_d and c) PDP.

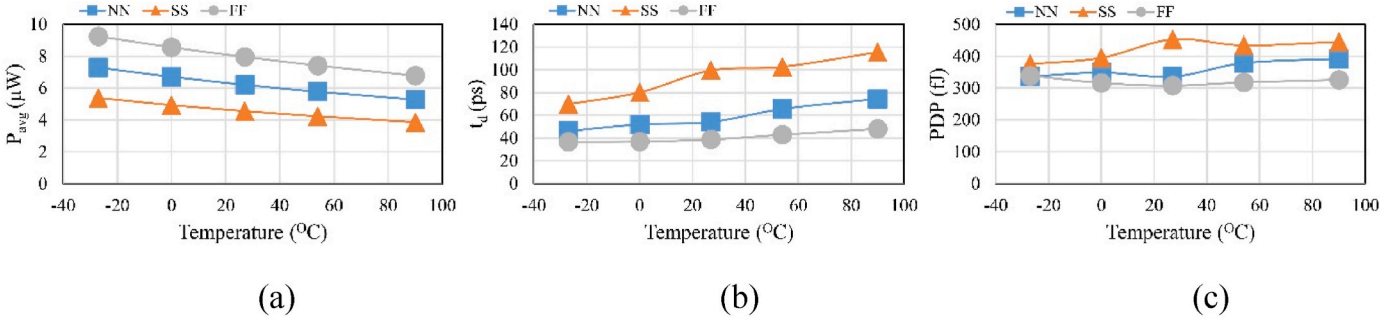

Fig. 14. Performance variation of 4:1 serializer with temperature at 1.1V a) P_{avg}, b) t_d and c) PDP.

corresponding value shows the simplicity of the proposed circuit. Additionally, a FOM of 65ns × fJ × μm^2 shows a robust design solution for the present design. Further, the jitter and BER are minimum in comparison to other designs. Based on the above data, the present design is found to be the best fit for any serializer interface.

7. Conclusions and further work

Coupled to a PDN, a 2:1 mux-latch is proposed for serializer interface. The present design achieves multiplexing and latch operation at the same time and eliminates enable inputs. This is completely different from the conventional designs, where enable inputs are necessary to

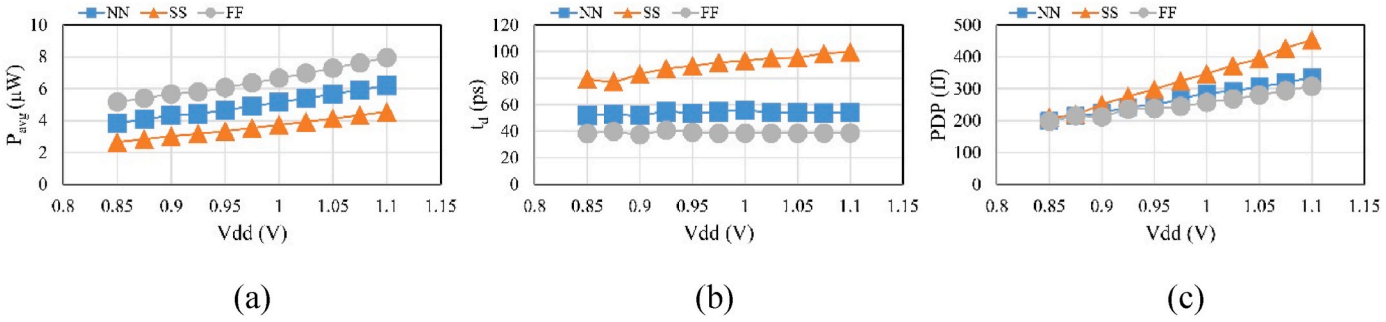

Fig. 15. Performance variation of 4:1 serializer with Vdd at 27^{O}C a) P_{avg}, b) t_d and c) PDP.

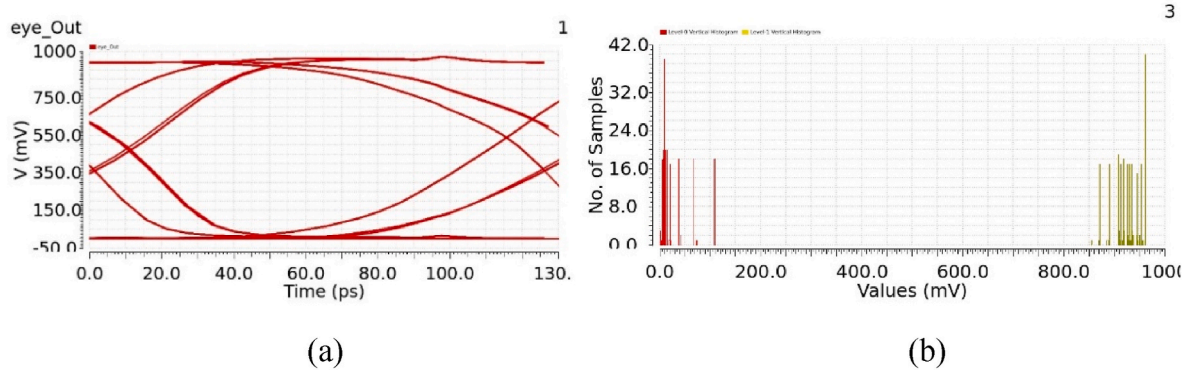

Fig. 16. Plot of a) output eye @ 4 GHz and b) histogram of 4:1 serializer.

Table 7
Output eye data in post-layout.

Parameters	Value
Threshold crossing Average (ps)	66.0
Threshold crossing stddev (ps)	52.3
Level 0 mean (mV)	30.3
Level 0 stddev (mV)	35.9
Level 1 mean (mV)	924.5
Level 1 stddev (mV)	31.4
Eye amplitude (mV)	894.2
Eye height (mV)	692.2
Eye Width (ps)	85.3
Eye S/N	13.3
Eye Rise Time (ps)	80.1
Eye Fall Time (ps)	83.4
Random Jitter (left) (ps)	2.3
Random Jitter (right) (ps)	0.31
Deterministic jitter (ps)	6.3

start latch operation. In addition to that, an analytical model is also derived to understand P_{avg}-t_d trade-off and suggests gate sizes to obtain an almost full voltage swing in 90-nm CMOS, 1.1 V Vdd and 6.25 GHz. Subsequently, the P_{avg}, t_d, PDP and FOM are noted to be 257.7 µW, 35 ps, 9 fJ and 65ns × fJ × µm^2. However, the performance variation at distinct corner is about 0.3 µW, 0.04 ps, 0.01 fJ and 0.2ns × fJ × µm^2, respectively, for 1^{O}C change in temperature. The corresponding change for 1 mV drop in Vdd is 0.4 µW, 0.03 ps, 0.01 fJ and 0.1ns × fJ × µm^2. The jitter is noted to be within 0.003–0.047 ps, while the white noise decreases at higher frequencies. Yet, the effective supply voltage V_P droops and oscillates with time as and when the CPU core draws 0–10 A, 20 A and 30 A in 10 ns. The Ldi/dt noise so generated introduces jitter in the output swing and t_d varies from 37.5 to 47.2 ps, respectively, for the said current ramps. Besides, the change in t_d due to AC noise is quite close to that of the DC and jitter is noted to vary lineary with AC first droop. However, [25,26]], have presented latches using C-element to identify incorrect state flipping of internal nodes due to particle strike and how to recover previous correct state. Nevertheless, the present work will be extended to understand the occurrence of above issue and to include necessary design modifications to avoid it.

Table 8
Performance comparison.

Ref.	[4]	[21]	[23]	This work	
Technology	90 nm	90 nm	90 nm	90 nm	
Feature	CML mux-latch	CML mux-latch	Mux dual latch	Mux-latch	
Function	2:1	2:1	2:1	2:1	4:1
Vdd (V)	1.1	1.1	1.1	1.1	1.1
Swing (mV)	933	1000	915	965	943
Clock Frequency (GHz)	6.25	6.25	6.25	6.25	4
Data Rate (Gbps)	13	13	13	13	8
Delay (ps)	74.6	52.2	44.1	35	54
Average Power (µW)	1954	1302	1847	257.7	6200
PDP (fJ)	145.8	68	81.5	9	335.8
FOM (ns × fJ × µm^2)	15,895	3352	1466	65	195
Jitter (ps)	4.1–7.54	0.53–8.7	0.11–0.35	0.003–0.47	0.3–2.3
Bit Error Rate	10^{-12}	10^{-12}	$<10^{-12}$	$<10^{-13}$	$<10^{-13}$
Area (mm^2)	0.77	0.577	0.244	0.0002	0.003

Author statement

The corresponding author is responsible for ensuring that the descriptions are accurate and agreed by all authors.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

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