Design Space Exploration of Interconnect Materials for Cryogenic Operation: Electrical and Thermal Analyses

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***Abstract*— With Copper (Cu) Interconnects causing performance bottleneck at single nanometer nodes due to increase in resistivity size effects viz., grain boundary scattering and surface scattering, there has always been scavenging for alternate interconnect materials. Although the Cu resistivity value decreases at cryogenic temperature, the problems continue to persist. In this work, we study three alternate interconnect materials specifically for 77K High Performance Compute applications. We select the materials based on their resistivity value at 77K for 7nm node computed using Fuchs-Sondheimer-Mayadas-Shatzkes (FS-MS) models. We analyze the delay of the interconnects, understand repeater insertion as a function of wire length, evaluate repeater count and energy at system level and perform IR drop analysis by showing through detailed analytical models that Ru, Rh and Al can provide appreciable improvements over Cu at 77K. The delay of interconnects reduces by 1-3.75% for Ru, 1.5-7.25% for Rh and 4.4-17.8% for Al across the BEOL stack while repeater counts decrease by 10%, 15% and 37% for Ru, Rh and Al respectively at 77K. We investigate thermal and reliability aspects of interconnect design including electromigration, Joule Heating and maximum allowed current densities again proving that Ru (9%), Rh (18%) and Al (63%) outperform Cu at 77K. Finally, we study the effects of various Low-k dielectric materials on the interconnect capacitance and thermal behavior for Cu as well as three alternate materials noting that, even though thermal conductivity of dielectrics decrease at 77K, the Joule Heating will not be as worse as one might expect.**

***Index Terms*— Alternate interconnects, cryogenics CMOS, dielectrics, electromigration, IR drop, Joule's heating, RC delay, repeater insertion.**

I. Introduction

INTERCONNECT technology has been dominated by copper (Cu) since its introduction due to its low bulk resistivity and has been the main work horse for CMOS based Very-Large Scale Integration (VLSI) [1]–[3]. The interconnect pitch scaling is a necessity for supporting denser transistor routing needs. With reduced wire thickness, the probability of electromigration and hence diffusion of copper atoms into the oxide or other dielectric increases posing reliability concerns. Hence, a barrier layer of higher activation energy and of suitable thickness was added around the copper interconnects and to increase the adhesivity, a liner material was also incorporated (Figure. 1) all of which led to surface scattering. At single nanometer nodes, the barrier/liner cannot be scaled without compromising the reliability of interconnects. While copper dimensions continue to scale down with the technology [4], it has been increasingly difficult to maintain the low resistance value of Cu due to increased grain boundary and surface scattering [5]. This consequential increase in *RC* delay has resulted in processor performance bottleneck at scaled nodes. Figure 2 shows the Elmore delay breakdown of top critical paths of a 64-bit Arm Processor across three nodes of 28nm Bulk CMOS and two generations of FinFETs at 14nm and 7nm [6]. It can be noticed that the wire delay becomes a significant part of the processor performance, dominating the gate delay at 7nm. Some of the approaches to extend copper to advanced nodes include (a) reducing barrier/liner thickness to increase copper cross-sectional area or using Self Formed Barriers [7], [8], (b) breaking the traditional dual damascene fill using via pre-fill [9], [10], (c) using thin liner materials to aid filling and compensate for thinner seeds [11], (d) Use of alternate Barrier Layers [12] (e) conformal deposition to avoid voiding [13]. However, all of these impact the reliability of the interconnects [14]. Although these methods can extend the current trend of Cu interconnect scaling for one-two more generations [15], the new materials research is well on its way to trying to replace copper.

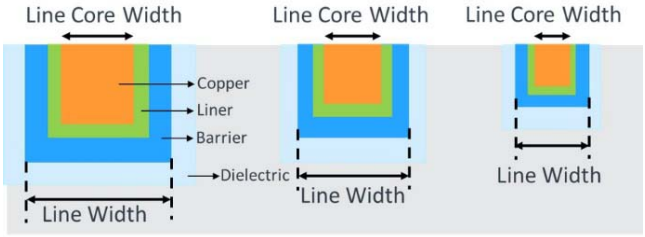

Fig. 1. Interconnect scaling across technology nodes, depicting reduction in the core width but the barrier/liner thickness remains constant.

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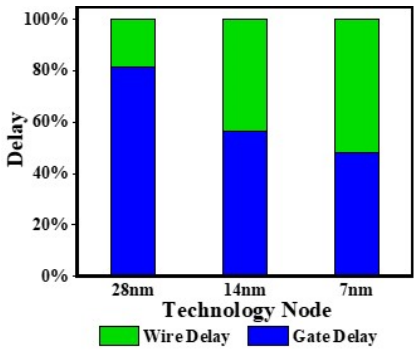

Fig. 2. Delay Breakdown of Critical Paths in a 64-bit Arm CPU.

Cryogenic CMOS has been studied for its power/performance benefits targeting High Performance Computing (HPC) applications [16], [17]. The interconnect problem landscape changes once we move to the cryogenic temperatures. With the decrease in the bulk resistivity of copper at lower temperatures, the RC delay reduces [6]. However, with the improvement in the device performance at low temperature due to increased transistor ON currents, the wire delay continues to dictate to the critical path timing. In this paper, we will present alternate interconnect materials that have been examined typically for room temperature and extend the study to cryogenic temperature (esp. 77K which might seem to be the optimal temperature for obtaining most device benefits). In this paper, comprehensive electrical and thermal analyses have been performed including but not limited to repeater analysis, IR drop analysis, electromigration, effects of dielectrics on interconnects and Joule's heating. All the analytical calculations are based on ASAP 7nm Predictive PDK [18], [19]. For the cryogenic device data, results from Gen-I (14nm) FinFET in [17] have been extrapolated for the 7nm node. The choice of interconnect materials is based on the Figure of Merit (product of bulk resistivity and mean free path) from ab initio techniques [20] and experimental data from the literature. The only available experimental data which captures the resistivity behavior of scaled interconnects at cryogenic temperature is for copper material [6]. Instead, we use calibrated analytical models to explore the suitability of the new materials at low temperature. For instance, the bulk resistivity data across temperature for the elemental metals is obtained from the literature [21]–[26] and used in conjunction with scattering parameters from ab-initio/experimental analyses at room temperature to estimate the resistivity at low temperature.

II. Low Temperature Interconnect Resistivity

A. Resistivity Models

The interconnect resistivity based on classical Fuchs-Sondheimer (FS) and Mayadas-Shatzkes (MS) model in its approximate form can be given in terms of bulk resistivity ρ_0, electron mean free path λ, interconnect width w_m, grain size D, specularity parameter p and grain boundary reflection coefficient R can be written as [27]:

$$\rho = \rho_0 + \rho_0\lambda\frac{3(1-p)}{4w_m} + \rho_0\lambda\frac{3R}{2D(1-R)} \quad (1)$$

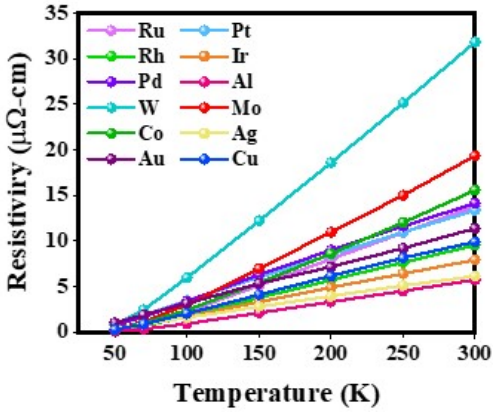

Fig. 3. Resistivity vs Temperature for different interconnect materials at 7nm Technology Node.

The second term in (1) represents the contribution of surface scattering with $p = 1$ indicating specular surface scattering and $p = 0$ indicating diffuse scattering. The third term in (1) represents the contribution of grain boundary scattering. We can notice that grain boundary scattering is inversely proportional to the grain size D and increases with increase in R, which can be viewed as probability of electron being back scattered by a grain boundary. One observation from (1) is that there will be no increase in the resistivity if either (i) there is specular reflection ($p = 1$) and/or (ii) grain boundary reflection coefficient $R = 0$. The pre-factor $\rho_0\lambda$ for both scattering mechanisms is determined by the electronic structure of a specific metal. The temperature dependence can be accounted by noting that fact that ρ_0 is a function of temperature.

B. Temperature Dependent Resistivity of Materials

The temperature dependent bulk resistivity of the different metals is obtained from published literature for list of most common alternative interconnects. In this work, we consider Ag, Al, Au, Co, Ir, Mo, Pd, Pt, Rh, Ru and W and compare with Cu. Due to the lack of 7nm experimental data on these interconnect materials across temperature, we use the bulk resistivity obtained from [21]–[26] and the models presented in (1) to estimate the resistivity on 7nm node. The interconnect dimensions for the 7nm BEOL is obtained from the ASAP 7nm Predictive PDK [18], [19]. The electron mean free path is obtained from [20], [27], [28]. The grain boundary reflection coefficients for these metals have been obtained from [6], [29]–[35]. A uniform value of specularity parameter of $p = 0.4$ has been used across all metals. The grain size is typically the smallest dimension of the interconnect. For the 7nm node [18], this is the 16nm after accounting for typical 1nm barrier/liner widths. The temperature dependence of resistivity is calculated with ρ_0 as a function of temperature T i.e., $\rho_0(T)$, while the scattering parameter, grain boundary reflection coefficient remaining constant w.r.t temperature. The calculated resistivity across temperature for these metals results in Figure 3.

The key takeaway from this analysis would be to look at the metals which provide lower resistivity than copper at

300K	Al	Ag	Ir	Rh	Cu	Au	Pt	Ru	Pd	Co	Mo	W
200K	Al	Ag	Ir	Rh	Cu	Au	Ru	Pt	Co	Pd	Mo	W
100K	Al	Ag	Ir	Rh	Cu	Ru	Co	Mo	Au	Pd	Pt	W
77K	Al	Rh	Ru	Ir	Ag	Cu	Co	Mo	Pd	Pt	Au	W

Fig. 4. Metals with resistivity better than Cu across temperature. (Green indicates lower value of ρ than Cu).

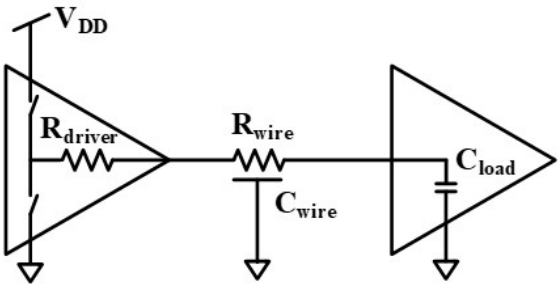

Fig. 5. Lumped Circuit Model for Single Stage Ring Oscillator.

a given temperature. The ordering of metals across four key temperatures is shown in Figure 4. We notice that even at room temperature, Al, Ag, Ir and Rh show better resistivity compared to copper which is coherent with the literature.

At 77K, Ru also shows improvements compared to Cu. Many prior works depict that Ru is better than Cu at room temperature as well, which can be subject of discussion as it depends on the interconnect dimensions, grain boundary reflection coefficients and many other factors. In our future analysis, we exclude Ir and Ag as the improvements compared to Cu is less than ∼10% at 77K and focus our discussion on Al, Rh, Ru and Cu. We include Ru in our 300K analysis to provide completeness. Henceforth, we will present a comparative study for these four metals for two temperatures of 300K (Room Temperature) and 77K (Cryogenic Temperature).

III. Electrical Analysis of Interconnects

A. Interconnect Delay

A direct implication of lower resistivity values is reduction in the interconnect RC delay. The capacitance of the interconnect being mainly influenced by the interconnect structure and the dielectric material, can be assumed to be equal for all the interconnect materials. Hence, the RC delay will follow the trend as shown in Figure. 3. A more appropriate analysis would be to study how the interconnects behave in conjunction with the circuit elements. For this, we consider a "Single Stage Ring Oscillator" structure where the interconnect is driven by a buffer and in turn drives a load. The equivalent lumped element model for this structure is shown in Figure. 5.

The delay τ of this configuration can be determined by Elmore's Delay model as:

$$\tau = 0.69R_{driver}C_{load} + 0.69R_{driver}C_{wire} + 0.69R_{wire}C_{load} + 0.38R_{wire}C_{wire} \quad (2)$$

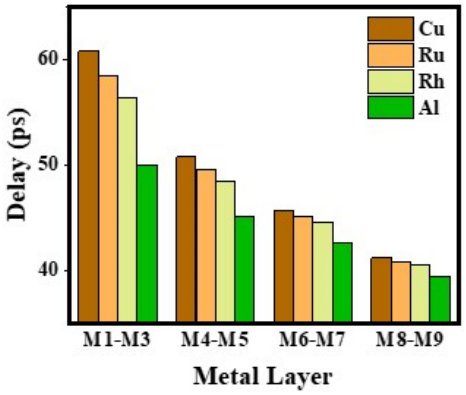

Fig. 6. Delay distribution across metal layers for different interconnect materials at 77K.

The driver resistance is the ON resistance of the buffer which can be estimated as

$$R_{ON} = \frac{t_{phl} + t_{plh}}{0.69 \cdot 2 \cdot C_L} \quad (3)$$

where t_{phl} and t_{plh} are high-low and low-high propagation delay of the buffer driving a load C_L. The wire resistance and capacitance depend on its dimensions. There are 4 variants of interconnects in the ASAP7 7nm predictive PDK. M1-M3, M4-M5, M6-M7, M8-M9, each having different width and thickness. Thus, for a wire of suitable length ($100\mu m$ in this case), four values of R_{wire} and C_{wire} are possible. The buffer resistance and capacitance for 7nm cells have been extrapolated from 14nm FinFET data for 77K in [17]. The delay for four metals under consideration is as shown in Fig. 6. The analysis shows improvements of 1-3.75% for Ru, 1.5-7.25% for Rh and 4.4-17.8% for Al across the BEOL stack, with higher improvement naturally for local interconnects (M1-M3) as they are most benefited by material change due to higher improvement in the resistivity size effects (scattering mechanisms).

B. Repeater Insertion

Repeater/buffer insertion is an effective technique for interconnect delay reduction which changes the delay dependence on length from quadratic to linear. The classical method to determine whether repeater insertion will reduce the interconnect delay is to determine if the sum of buffer delays and the shorter interconnect segments is smaller than the long unsegmented wire delay. The optimal number of repeaters that needs to be inserted depends on the ratio of interconnect delay to the gate delay and can be mathematically derived using Elmore delay models which results in well-known formulation:

$$n_{opt} = \sqrt{\frac{R_{wire}C_{wire}}{2.3R_0C_0}} \quad (4)$$

where R_{wire} and C_{wire} are interconnect resistance and capacitance, R_0 and C_0 are the resistance and output capacitance of unit sized repeater. The optimal number of repeaters is determined as a function of net length across the BEOL stack

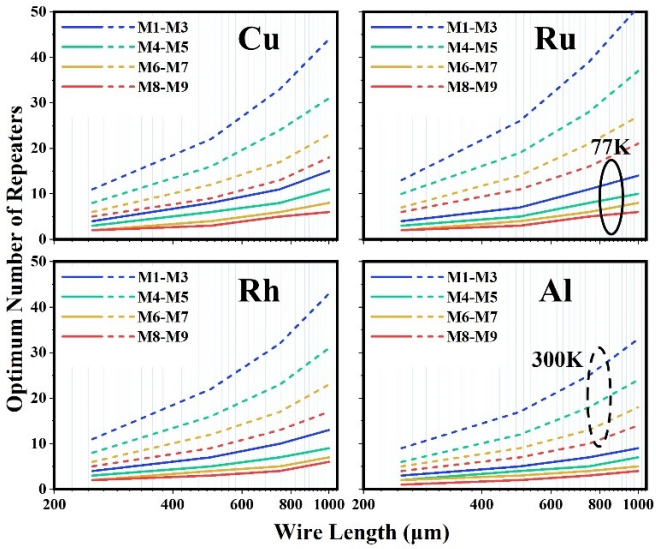

Fig. 7. Optimum Repeater Count as function of wire length for Cu, Rh, Ru & Al interconnects, at 300K and 77K across BEOL.

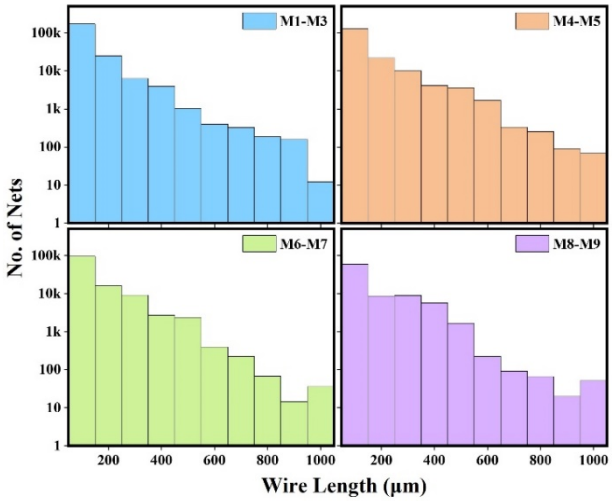

Fig. 8. Net length histogram of processor design across the BEOL stack.

for four metals under study at two temperatures of 300K and 77K and is shown in Figure 7. The repeater count is lower at 77K compared to 300K across the BEOL layers for all materials due to reduction of wire resistivity with decrease in temperature. At 300K. the Ru repeater count is slightly higher than Cu repeater count due to higher RC delays of Ru interconnects based on analysis in section II. Al shows highest improvements with repeater count reducing between 33-40% (22-25%) across BEOL layers compared to Cu at 77K (300K) for $1000\mu m$ wires.

It would be interesting to understand how the repeater count scales with temperature and materials at a system level. For this, we consider a processor design which has completed auto place and route flow in 7nm comprising of approximately 700k gates. This is not a routing constrained design meaning the track layer resources are well in abundance compared to actual routing required. The net length distribution for such a design is shown in Figure. 8. Any net length higher

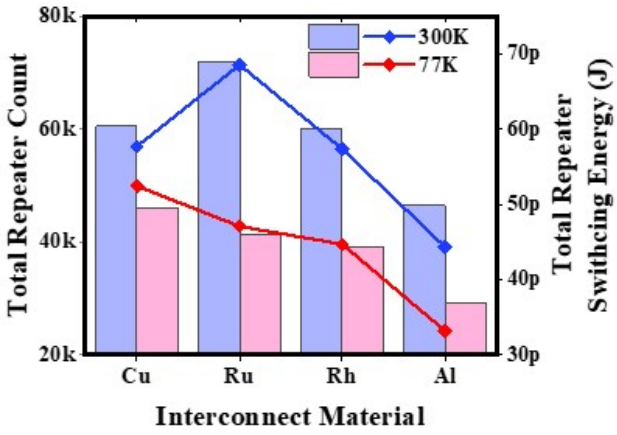

Fig. 9. Total Repeater Count (bar graphs) along with total repeater switching energy (line graph) at $V_{DD} = 0.8V$ at system level for different interconnect materials at 300K and 77K.

than $1000\mu m$ is considered as an outlier and not accounted for in the further analysis. For this design, there is only 1 outlier in M8-M9 category. From the two histograms, we can calculate the average number of repeaters at the system level as shown in Figure. 9. In our previous analysis, all the repeaters are unit repeaters. Here, we use the output capacitance of the unit repeaters to calculate the total repeater switching energy (right axis of Figure 9).

The total repeater count for Ru is 10% lower, Rh is 15% lower and Al is 37% lower compared to Cu at 77K and the total repeater switching energy follows the same trend. Thus, at 77K we see benefit at the system level in power, performance and area when using Ru, Rh and Al as alternative interconnect materials. This analysis may differ if the design is routing constrained or if it is macro intense. Alternately, if the design is congestion constrained (high utilization and cell density $> 70\%$), then addition of repeaters might be difficult and APR tools tend to upsize other combinational cells which deviates from this analysis.

C. IR Drop

One of the key challenges of building a Power Distribution Network (PDN) is minimizing the IR drop along with reduction of Simultaneous Switching Noise (SSN). Increase in chip dimensions and chip current drain, reduction in supply voltage and shrinking interconnect dimensions only add complexity to the PDN design. In this part, we analyze how the interconnect materials can aid in reducing IR drop.

Consider a PDN which is peripheral wire bonded (chip power is fed through bonding pads at chip periphery) with a mesh structure connected to an equipotential outer ring as shown in Figure 10. The 3D visualization and the equivalent resistive network modelling is also shown. If the power dissipation is uniform across the chip, the worst case IR drop is from the center of the chip to the equipotential outer ring [36]. The percentage IR drop δ, given the metal coverage Cov (defined as ratio of power distribution metal area to the chip area) is given by (5) [36].

$$\delta = \frac{m_p P_{tot} \rho}{16 V_{DD}^2 t_m} \tag{5}$$

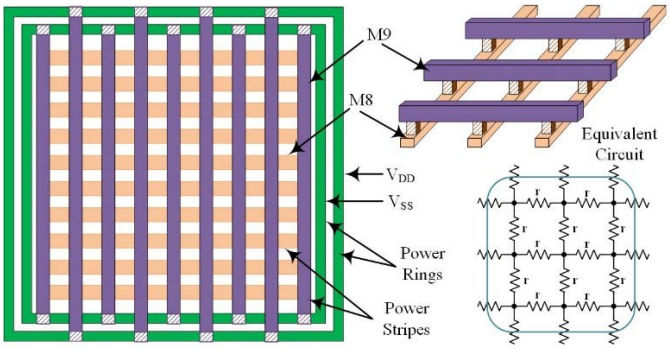

Fig. 10. Model PDN with outer power ring and inner mesh structure built on global layers (M8-M9) along with 3D image and equivalent resistive model.

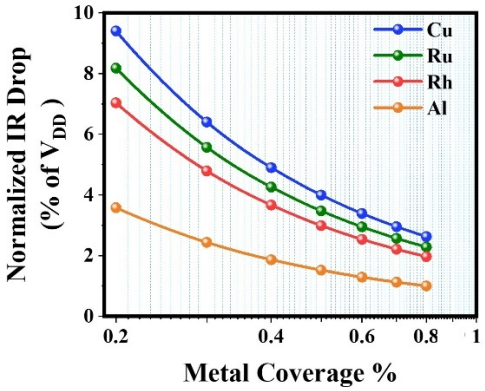

Fig. 11. Normalized IR drop as function of metal coverage Cov for four interconnect materials at 77K.

where m_p is given by

$$m_p = \frac{1+\sqrt{1-Cov}}{Cov} \tag{6}$$

$$Cov = \frac{A_{power-dist}}{A_{chip}} \tag{7}$$

P_{tot} is the total power dissipation of the chip, ρ is the metal resistivity, V_{DD} is the supply voltage and t_m is the interconnect thickness. Figure. 11. shows the normalized IR drop for the four interconnect materials at 77K as a function of the metal coverage. Note that from (5), if the other design parameters are kept constant, the IR drop becomes purely a function of the resistivity of the interconnect material. Also note that the IR drop starts to saturate at higher metal coverage, and it is not feasible to get a metal coverage beyond 80% (typically) due to metal spacing rules. This analysis also holds good for area-array bonding system, where the pad will at the center of the cutting boundary in the equivalent circuit.

IV. Thermal and Reliability Analysis

A. MTTF and Electromigration Due to Diffusion

The electronic industry uses mean-time-to-failure (MTTF) analysis to predict the lifetime of a device. The failure due to electromigration is characterized by Black's equation:

$$MTTF = A\frac{1}{j^n}\exp\left(\frac{E_a}{kT}\right) \tag{8}$$

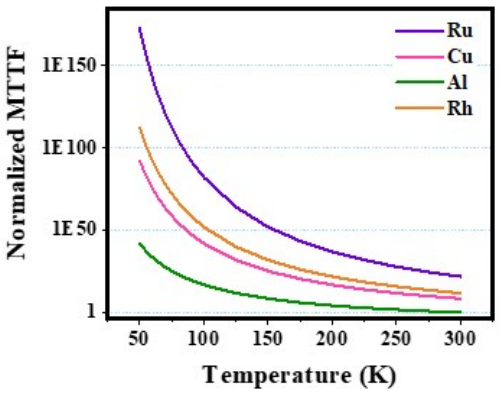

Fig. 12. Normalized MTTF vs Temperature for different interconnect materials.

A is the cross-section area for diffusion, j is the current density, n is the power factor (varies between 1 and 2), E_a is the activation energy of atomic diffusion in electromigration, k is the Boltzmann's constant, T is the temperature. The activation energy depends on the type of diffusion the metal undergoes (grain-boundary or surface). The activation energies for different materials under consideration is found in literature [37]–[40]. Assuming the current densities are same in all the materials, the normalized MTTF for the four materials is shown in Figure 12. It can be observed that Ru, with highest activation energy of 1.8eV has the highest MTTF across temperature. The room temperature reliability concerns of aluminum will get addressed at cryogenic temperature. The applicability of Black's equation (which was originally developed based on rate of forming a void in Al), to other materials is still a point of discussion and deserves careful examination.

B. Current Density and MTTF

The current flow in the interconnects cause self-heating or Joule Heating which limits the maximum allowable current density in order to limit the temperature increase. Also, the MTTF has exponential dependence on inverse of the metal temperature as seen from (8). An analytical model for interconnect temperature profile using heat diffusion equations in a steady state system (such as one shown in figure 13) leading to self-consistent solutions were demonstrated in [41]. This leads to relation between current density j_{rms} and rise in temperature due to self-heating ΔT_{SH} as

$$j_{rms}^2 = \frac{\Delta T_{SH} K_{ins} W_{eff}}{t_{ins} t_m w_m \rho} \tag{9}$$

$$\Delta T_{SH} = T_m - T_{ref} \tag{10}$$

where K_{ins} is the thermal conductivity of the dielectric, t_m is the metal thickness, w_m is the metal width, t_{ins} is the total thickness of the underlying dielectric, ρ is the resistivity of the metal at the given temperature, W_{eff} is the effective width of the metal line considering quasi-2D heat conduction. Assuming the rise in temperature is constant for all the interconnect materials, we calculate the maximum j_{rms} at two temperatures and normalize it to 300K Cu interconnect (figure 14). It is interesting to observe that even though

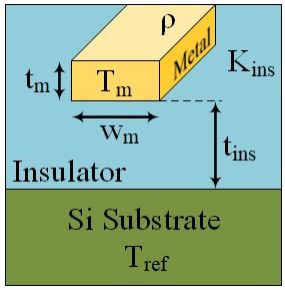

Fig. 13. Dielectric-Interconnect system showing different variables, with substrate at temperature T_{ref} and metal at T_m.

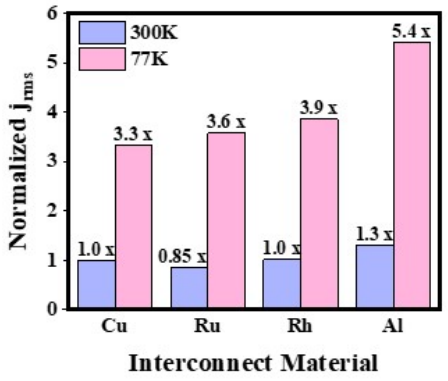

Fig. 14. Maximum RMS current density j_{rms} for different interconnect materials normalized to 300K Cu value.

Al has lower EM activation energy, it can sustain >1.6x current density than Cu does at 77K for the same increase in interconnect temperature.

C. Joule Heating Slope

We can also examine the increase in temperature as a function of current for different interconnect materials. Figure 15 shows rise in temperature ΔT as a function of I^2 for cryogenic system at 77K. The slope of this curve B (called Joule Heating Slope [14]) denotes rate of change of temperature as function of current. B is a function of the interconnect dimensions, resistivity of the interconnect material and the thermal conductivity of the surrounding dielectric. Higher the value of B, higher is the rise in temperature ΔT. We see that for a given current (and given current density assuming interconnect dimensions are same across all materials), Al has the least rise in temperature, followed by Rh, Ru and Cu at 77K.

V. Effect of Dielectric Materials

The Inter Layer Dielectric (ILD) material plays a key role in depicting the interconnect behavior. The choice of ILD materials impact the value of interconnect capacitance and hence the RC delay, reliability in terms of TDDB (time dependent dielectric breakdown), heat dissipation and interconnect reliability, facilitating diffusion of interconnect metal ions and electromigration etc., To complete the study, we look at two important aspects of dielectric materials (i) Interconnect Capacitance (Electrical) and (ii) Joule Heating (Thermal).

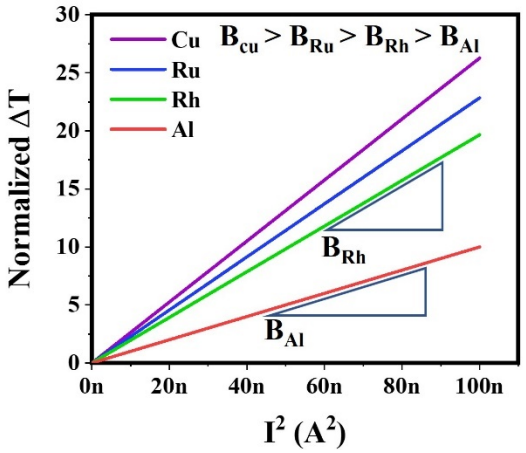

Fig. 15. Normalized increase in temperature ΔT versus I^2 at 77K for different interconnect materials.

A. Interconnect Capacitance

The semiconductor industry is exploring new Low-κ dielectric materials for better RC value to increase speed and to reduce interconnect cross-talk and bit-line capacitance for the memory chips. Dielectric constant being measure of electric polarizability of a material, the most obvious choice is a material with fewer polar chemical groups. Other desirable properties include good thermal stability, good adhesion to substrate, high dielectric breakdown, low charge trapping, chemical inertness etc., In this work we will focus on conventional SiO_2 ($\kappa = 3.9$), Fluorosilicate Glass/FSG ($\kappa = 3.5$), Hydrogen Silesquioxanes/HSQ ($\kappa = 3$) and Carbon-Doped Oxide3/CDO3 ($\kappa = 2.7$).

The interconnect capacitance as a function of dielectric constant and interconnect dimensions for sub nanometer nodes is effectively modelled by analytic expressions from [42] as:

$$C = \begin{cases} \varepsilon \left[\dfrac{w - \frac{t}{2}}{h} + \dfrac{2\pi}{ln\left(1 + \frac{2h}{t}\sqrt{\frac{2h}{t}\left(\frac{2h}{t} + 2\right)}\right)} \right] & w \geq \dfrac{t}{2} \\ \varepsilon \left[\dfrac{w}{h} + \dfrac{\pi\left(1 - 0.0543\frac{t}{2h}\right)}{ln\left(1 + \frac{2h}{t}\sqrt{\frac{2h}{t}\left(\frac{2h}{t} + 2\right)}\right)} + 1.47 \right] & w < \dfrac{t}{2} \end{cases} \tag{11}$$

where w and t width and thickness of the interconnect, and h is the distance from the ground plane. The wire capacitance per unit length as a function of the aspect ratio for different dielectric materials is shown in Figure 16.

B. Joule Heating and Low-k Dielectrics

The low- κ dielectric materials can further exacerbate thermal effects owing to their low thermal conductivity compared to SiO_2 [43]. Further at cryogenic temperature, the thermal conductivity of low-κ materials decrease compared to 300K, which increases the Joule Heating Slope ($B \propto {}^{1}/_{K_{ins}}$).

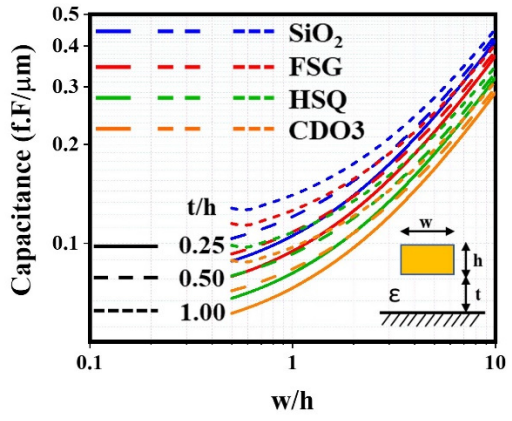

Fig. 16. Interconnect capacitance per unit length as function of wire aspect ratio for different dielectric materials.

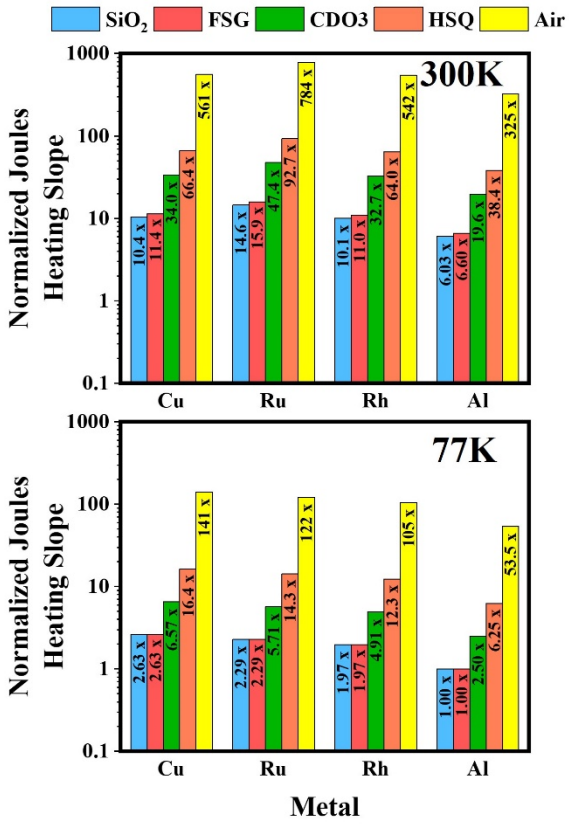

Fig. 17. Joule Heating Slope of various interconnect materials and ILDs normalized to Al with SiO_2 as dielectric at 77K.

We determine the Joule Heating Slope of the four interconnect materials under consideration for the ILDs mentioned above at 300K and 77K. We also include air as dielectric material since air-gaps are widely used to reduce capacitance.

The figure 17 shows the Normalized Joule Heating Slope for different interconnect materials and ILDs. Although the thermal conductivity of ILDs decrease with temperature as recorded in Table I, the increase in the conductivity of interconnect materials results in a net reduction of self-heating at cryogenic temperature.

TABLE I
THERMAL CONDUCTIVITY OF ILDS AT 300K AND 77K

ILD	K_{ins} (300K) (W/mK)	K_{ins} (77K) (W/mK)	Ref
SiO_2	1.40	0.5	[44]
FSG	1.28	0.5	[45]
CDO3	0.43	0.2	[45]
HSQ	0.22	0.08	[46]
Air	0.026	0.00934	[47]

TABLE II
POWER PERFORMANCE AREA BENEFITS OF ALTERNATE INTERCONNECT MATERIALS AT 77K AND INTEGRATION CHALLENGES

Metal	Power*	Area*	Perf[++]				Challenges
			L1	L2	L3	L4	
Cu	1x	1x	1x	1x	1x	1x	Exponential increase in size effects leading to higher resistance of interconnects at advanced nodes.
Ru	0.93x	0.89x	0.96x	0.97x	0.98x	0.99x	Direct metal etch of Ru at small dimensions is impacted by the growth of an oxidized layer, leading to an etch stop in the smallest features [48].
Rh	0.91x	0.85x	0.93x	0.95x	0.97x	0.98x	Poor adhesion to dielectric, expensive, corrosion or polish non-uniformity limits the yield [14].
Al	0.76x	0.63x	0.82x	0.88x	0.93x	0.95x	Subtractive etch at fine pitch is difficult to attain making it harder to scale.

VI. CONCLUSION

In this paper we have thoroughly studied the various aspects of a CMOS system from the interconnects perspective-both electrical and thermal for three potential alternative materials to copper mainly focusing on cryogenic systems at 77K. Exhaustive analytical models have been used to demonstrate the suitability of Ru, Rh and Al for single nanometer nodes at 77K. The initial investigation of $\rho_0\lambda$ to select suitable alternatives paved path to delay analysis followed by repeater modelling and IR drop study.

Further, the thermal and reliability aspects of electromigration, self-heating and maximum allowed current densities all demonstrated that Al is best suitable replacement for cryogenic systems. The prevailing reliability concerns in Al interconnects will be addressed by lower EM at low temperature. Albeit some process challenges, there is power, performance and area improvements at 77K as summarized in Table II.

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